BAT32G135B Datasheet

Ultra-low power 32-bit microcontrollers based on ARM® Cortex®-M0+

64KB Flash, analog functions, timers and communication interfaces.

V0.5.3

Features

- **Ultra-low power consumption technology:**
  - Operating voltage: 1.8V to 5.5V
  - Operating temperature: -40℃ to 105℃
  - Low power modes: sleep mode and deep sleep mode
  - Operating power consumption: 73μA/MHz@64MHz
  - Power consumption in deep sleep mode: 1μA
  - Operation in deep sleep mode +32.768K+RTC: 1.15μA
- **Core:**
  - ARM® 32-bit Cortex®-M0+ CPU
  - Operating frequency: 32KHz to 64MHz
- **Memory:**
  - 64KB Flash Memory
  - 1.5KB dedicated data Flash Memory
  - 8KB SRAM Memory with parity check
- **Power and reset management:**
  - Power-on reset (POR)
  - Low voltage detection (LVD) (settable threshold voltage)
- **Clock management:**
  - Internal 64MHz high-speed oscillator
  - Internal 15KHz low-speed oscillator
  - Supports 1MHz~20MHz external oscillators
  - Supports 32.768KHz external oscillators
  - 1-channel PLL with up to 64MHz system clock
- **Multiplier module:**
  - Supports 32-cycle and 32-bit multiplication.
- **EDMA controller:**
  - Interrupt triggered startup
  - Selectable transfer modes (Normal transfer mode, Repeat transfer mode, Block transfer mode and Chain transfer mode)
  - The source/target fields for transfer can be optionally selected from the full address space range.
- **Analog peripherals:**
  - 12-bit ADC converter with 1.42Msps conversion rate, 35 external analog channels, internal optional PGA0/1 output as conversion channels, with a temperature sensor supporting for single-channel/multi-channel scan conversion mode. Conversion range: 0 to positive V_{REF}
  - 2-channel Comparator (CMP), input source selectable, reference voltage selectable from external reference voltage or internal reference voltage
  - 2-channel Programmable Gain Amplifier (PGA) with 4/8/10/12/14/16/32x gain selection
- **Input/output ports:**
  - I/O ports: 29~45
  - N-channel open drain, internal pull-up/down switching
  - Internal key interrupt detection
  - Internal clock output/buzzer output controller
- **Serial 2-wire debugger (SWD)**
- **Timers:**
  - 16-bit timer: 8 channels
  - 15-bit interval timer: 1x
  - Real Time Clock (RTC): 1x (with perpetual calendar, alarm function, and clock correction)
  - Windowed watchdog timer (WWDT): 1x
  - SysTick timer
- **Interfaces:**
  - 2 serial communication units: freely configurable as 3-channel standard UART or 6-channel SPI or 6-channel simplified I^2C
  - Standard SPI: 1 channel (8-bit and 16-bit supported)
  - Standard I^2C: 1 channel
  - IrDA: 1 channel
- **Safety functions:**
  - Complies with IEC/UL 60730 standards
  - Reports abnormal storage access errors
  - Supports RAM parity check
  - Supports hardware CRC
  - Supports SFR guard and avoids misoperation
  - 128-bit unique ID number
  - Flash Level 2 protection in the debug mode

- **Linkage controller:**
  - It can link event signals to realize the linkage of peripheral functions
  - 15 input events and 4 trigger events

(Level1: can only perform a flash full-scale erase and cannot read or write. Level2: The emulator connection is invalid and cannot operate on the flash.)

- **Package:**
  - 48LQFP, 40QFN, 32LQFP

1 Overview

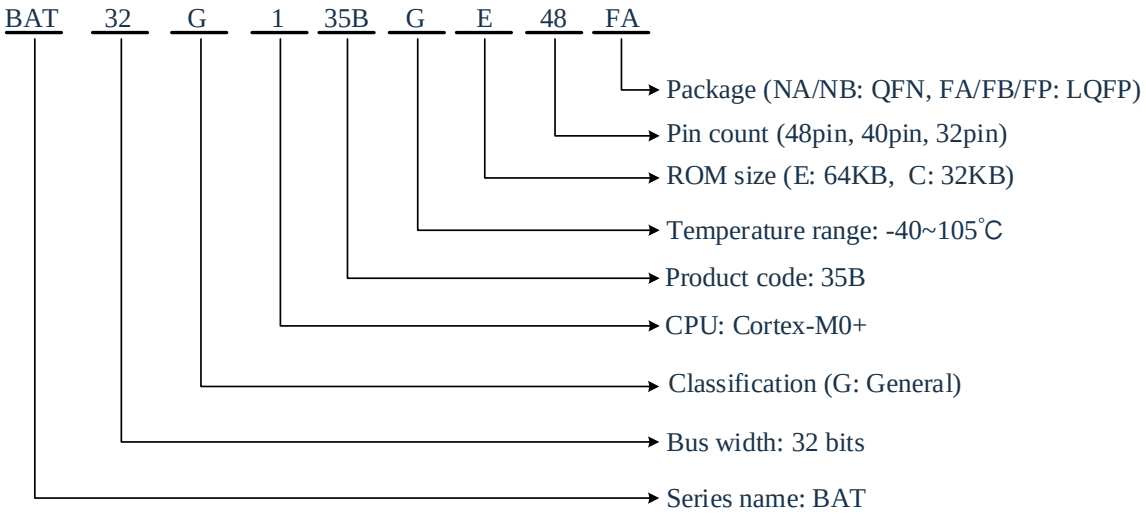
1.1 Brief Introduction

The ultra-low power BAT32G135B features a high-performance ARM® Cortex®-M0+ 32-bit RISC core, operating up to 64MHz, with 64KB Flash, 8KB SRAM, and 1.5KB Data Flash. This product integrates multiple standard interfaces including I^2C, SPI, UART, and LIN. It also includes a 12-bit A/D converter, temperature sensor, and comparator, with a programmable gain amplifier (PGA). The 12-bit A/D converter can be used for collecting external sensor signals, reducing system design costs. The integrated temperature sensor provides real-time monitoring of the external environment temperature. The built-in comparator supports both high-speed and low-speed operating modes. In high-speed mode, it can be used for control feedback in high-speed motor operations, while in low-speed mode, it is suitable for battery monitoring. The BAT32G135B also features an 8-channel 16-bit timer module and is equipped with an EPWM control circuit. Combined with the timer, it enables control of a DC motor or two stepper motors.

Additionally, the microcontroller offers excellent low-power performance, supporting both sleep and deep sleep modes, providing flexible design options ideal for battery-powered low-power devices. Furthermore, the integration of an event-linked controller enables direct connection between hardware modules without CPU intervention. This approach provides faster response times than using interrupts and lowers CPU activity frequency, thereby extending battery life.

These features make the BAT32G135B microcontroller series highly suitable for applications in energy storage systems, battery packs, motor control, security, and power industries.

1.2 Product Model List



BAT32G135B product list:

Product code	Package	Flash Memory	Dedicated data Flash Memory	SRAM
BAT32G135BGE32FP	32-pin plastic package LQFP (7x7mm, 0.8mm pitch)	64KB	1.5KB	8KB
BAT32G135BGE40NB	40-pin plastic package QFN (5x5mm, 0.4mm pitch)			
BAT32G135BGE48FA	48-pin plastic package LQFP (7x7mm, 0.5mm pitch)			

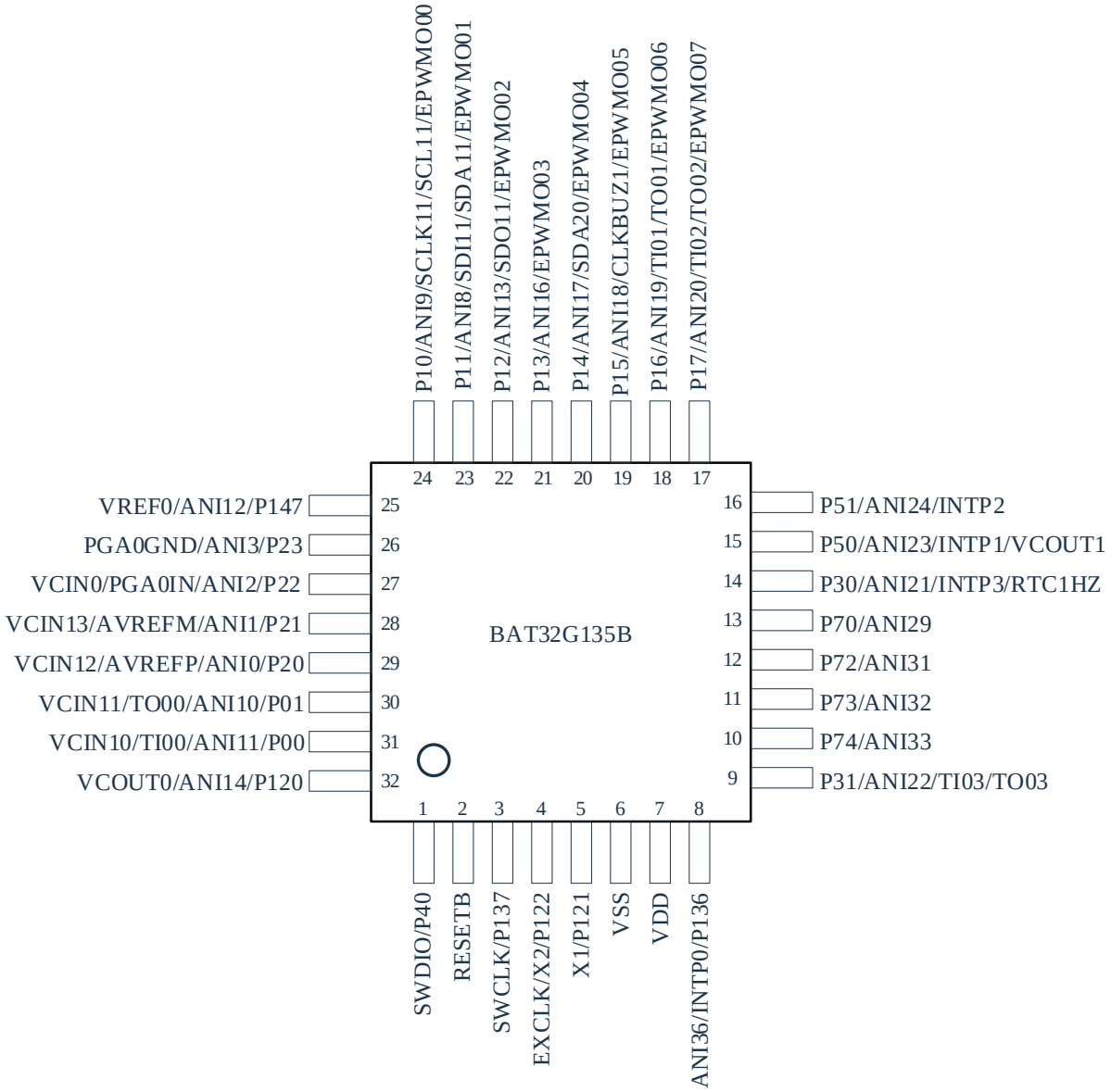
BAT32G135B product selection table:

Part No.	Core	Main frequency (MHz)	Min. operating voltage (V)	Max. operating voltage (V)	Code Flash (kB)	SRAM (kB)	Data Flash (kB)	DMA	GPIO	12-bit ADC	CMP	PGA	Universal timer (16bit)	RTC	WDT	UART	SPI	IIC bus	IrDA bus	Hardware multiplier	Hardware divider	Package
BAT32G135B GE32FP	M0+	64	1.8	5.5	64	8	1.5	24	29	25+3	2	1	8	1	1	3	1+3	1+3	1	Y	Y	LQFP32
BAT32G135B GE40NB	M0+	64	1.8	5.5	64	8	1.5	24	37	28+4	2	2	8	1	1	3	1+4	1+4	1	Y	Y	QFN40
BAT32G135B GE48FA	M0+	64	1.8	5.5	64	8	1.5	24	45	35+4	2	2	8	1	1	3	1+5	1+5	1	Y	Y	LQFP48

1.3Top View

1.3.1 BAT32G135BGE32FP

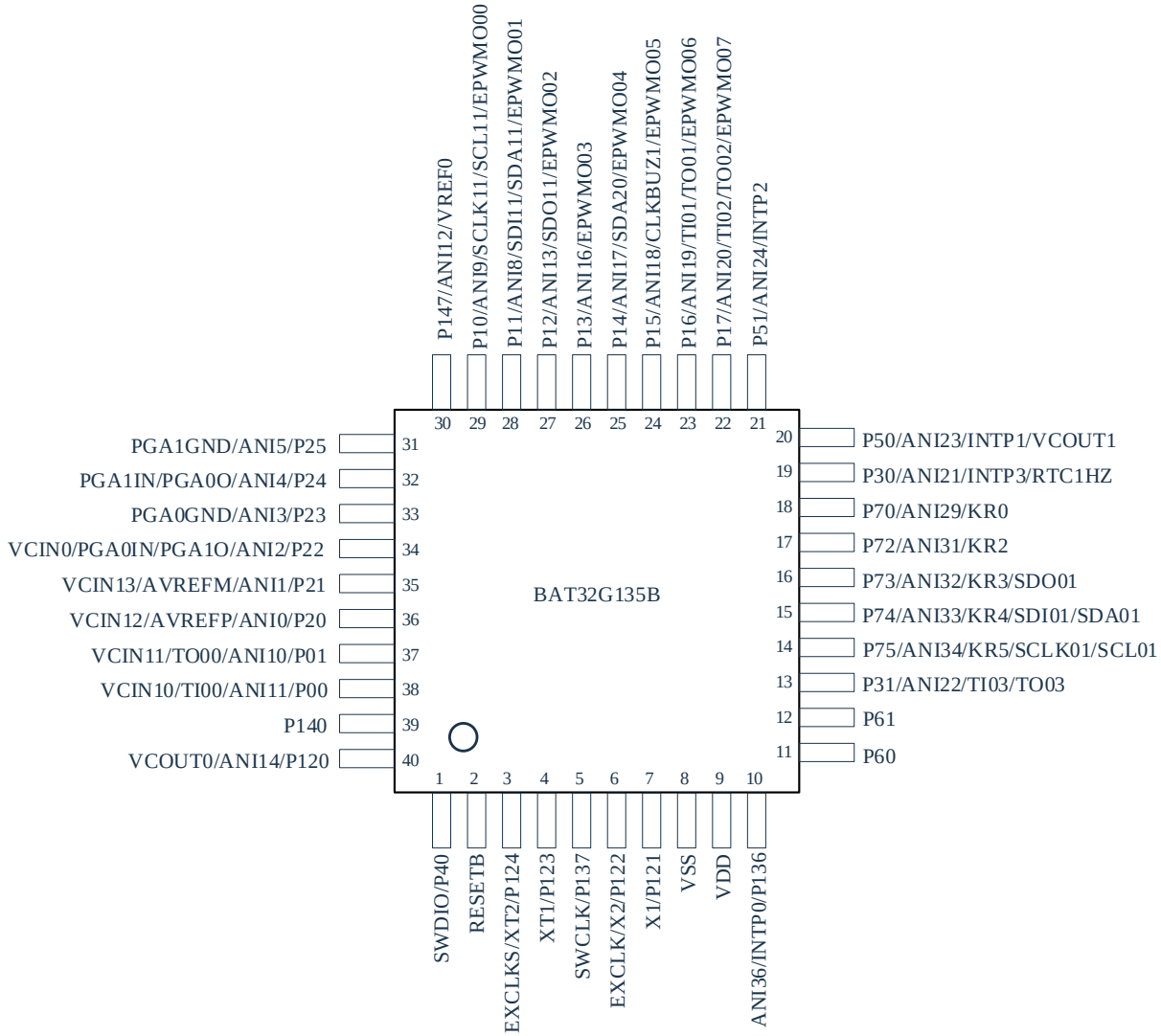
- 32-pin plastic package LQFP (7x7mm, 0.8mm pitch)



Note: The unmarked digital functions of the pins in the diagram can be configured. Please refer to section 4.1 for details.

1.3.2 BAT32G135BGE40NB

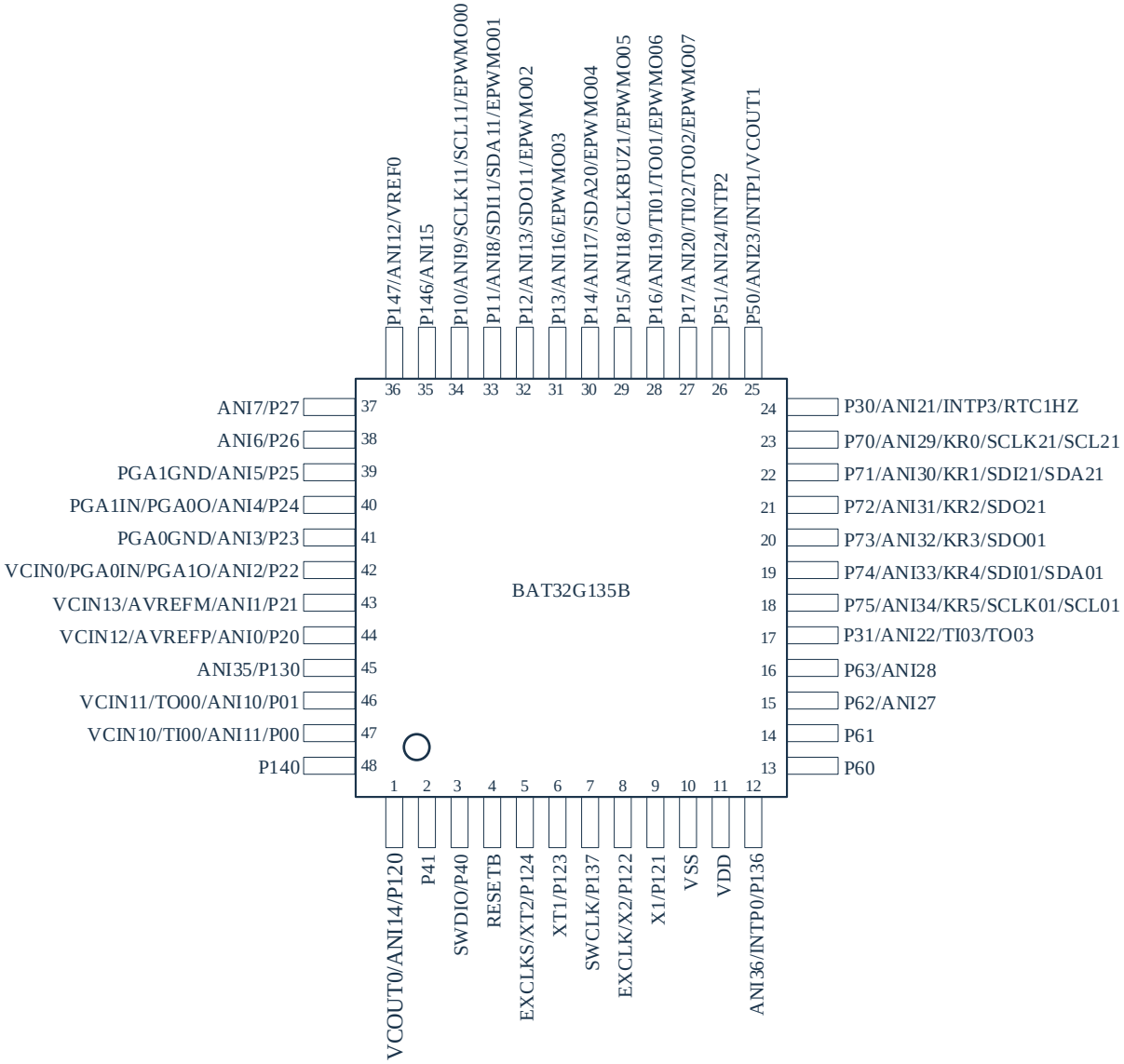
- 40-pin plastic package QFN (5x5mm, 0.4mm pitch)



Note: The unmarked digital functions of the pins in the diagram can be configured. Please refer to section 4.1 for details.

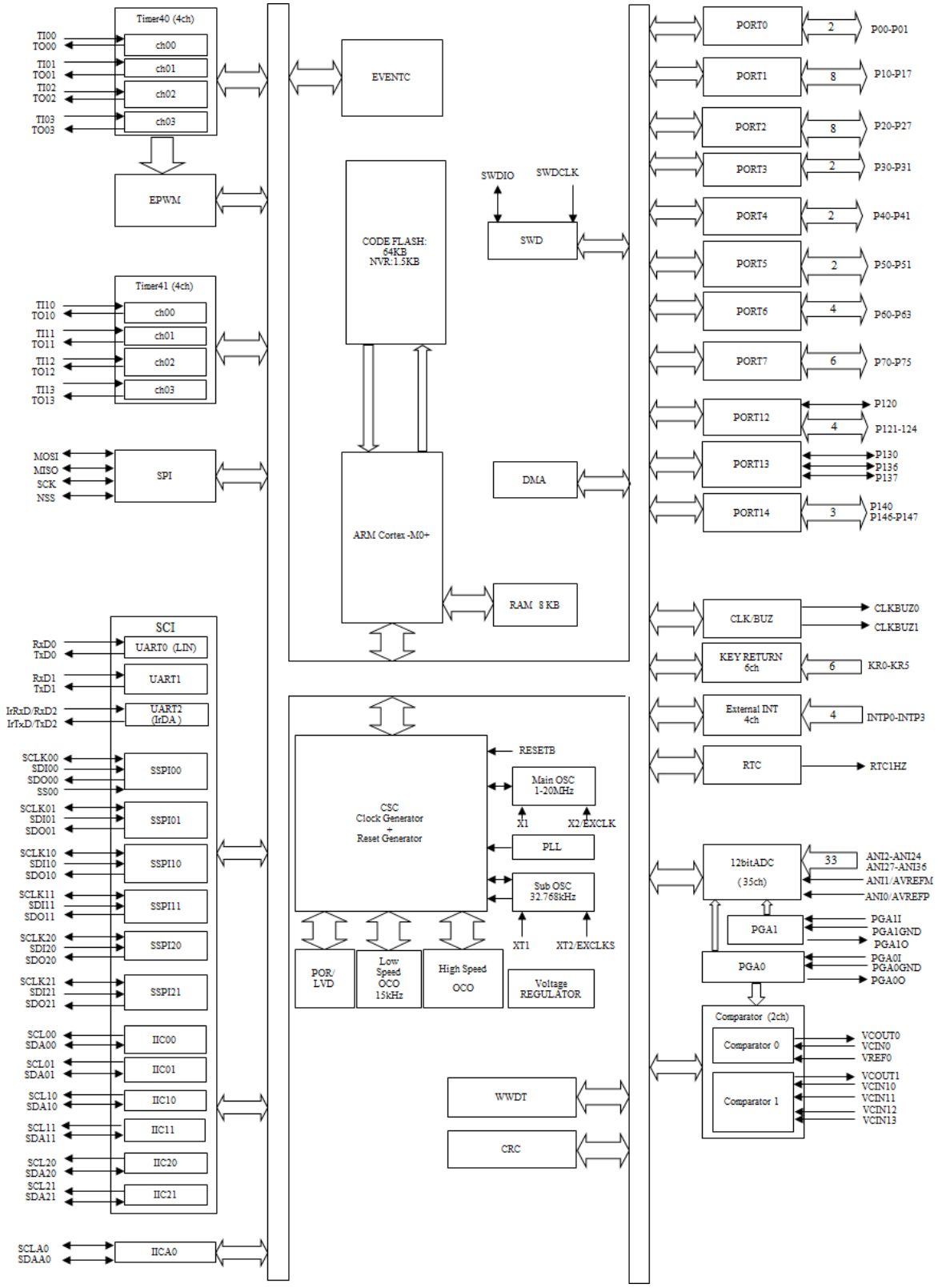
1.3.3 BAT32G135BGE48FA

- 48-pin plastic package LQFP (7x7mm, 0.5mm pitch)



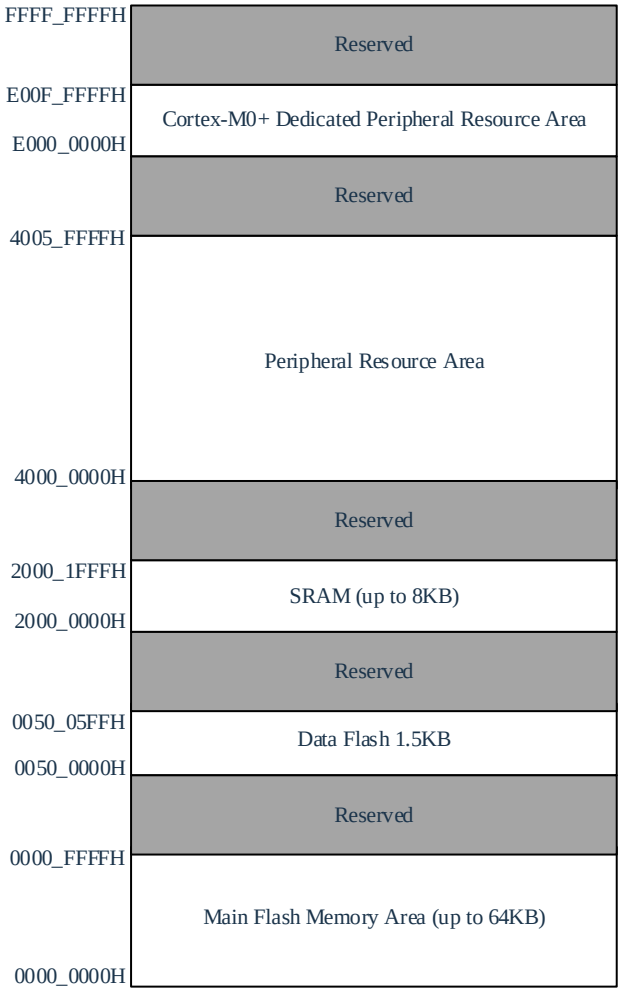
Note: The unmarked digital functions of the pins in the diagram can be configured. Please refer to section 4.1 for details.

2 Product Block Diagram



The above diagram shows the block diagram of a 48-pin product, some functions are not supported for products with less than 48 pins.

3 Memory Map


FFFF_FFFFH
Reserved
E00F_FFFFH
Cortex-M0+ Dedicated Peripheral Resource Area
E000_0000H
Reserved
4005_FFFFH
Peripheral Resource Area
4000_0000H
Reserved
2000_1FFFH
SRAM (up to 8KB)
2000_0000H
Reserved
0050_05FFH
Data Flash 1.5KB
0050_0000H
Reserved
0000_FFFFH
Main Flash Memory Area (up to 64KB)
0000_0000H

4 Pin Functions

4.1 Port Functions

Table 4.1.1

Port name	Alternate function	Digital output function setting register pxxcfg[3:0]	Digital input function setting register xxxPCFG[5:0]	With or without function		
				LQFP48	QFN40	LQFP32
RESETB	RESETB	-	-	●	●	●
P00	GPIO	00H	00H	●	●	●
	ANI11	00H	00H	●	●	●
	VCIN10	00H	00H	●	●	●
	TI00	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P01	GPIO	00H	00H	●	●	●
	ANI10	00H	00H	●	●	●
	VCIN11	00H	00H	●	●	●
	TO00	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P10	GPIO	00H	00H	●	●	●
	ANI9	00H	00H	●	●	●
	SCLK11	00H	00H	●	●	●
	SCL11	00H	00H	●	●	●
	EPWMO00	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P11	GPIO	00H	00H	●	●	●
	ANI8	00H	00H	●	●	●
	SDI11	00H	00H	●	●	●
	SDA11	00H	00H	●	●	●
	EPWMO01	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P12	GPIO	00H	00H	●	●	●
	ANI13	00H	00H	●	●	●
	SDO11	00H	00H	●	●	●
	EPWMO02	00H	00H	●	●	●

	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P13	GPIO	00H	00H	●	●	●
	ANI16	00H	00H	●	●	●
	EPWMO03	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P14	GPIO	00H	00H	●	●	●
	ANI17	00H	00H	●	●	●
	SDA20	00H	00H	●	●	●
	EPWMO04	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P15	GPIO	00H	00H	●	●	●
	ANI18	00H	00H	●	●	●
	CLKBUZ1	00H	00H	●	●	●
	EPWMO05	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P16	GPIO	00H	00H	●	●	●
	ANI19	00H	00H	●	●	●
	TI01	00H	00H	●	●	●
	TO01	00H	00H	●	●	●
	(SPIMOSI)	00H	00H	●	●	●
	EPWMO06	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P17	GPIO	00H	00H	●	●	●
	ANI20	00H	00H	●	●	●
	TI02	00H	00H	●	●	●
	TO02	00H	00H	●	●	●
	(SPIMISO)	00H	00H	●	●	●
	EPWMO07	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P20	GPIO	00H	00H	●	●	●
	ANI0	00H	00H	●	●	●
	AVREFP	00H	00H	●	●	●
	VCIN12	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P21	GPIO	00H	00H	●	●	●

	ANI1	00H	00H	●	●	●
	AVREFM	00H	00H	●	●	●
	VCIN13	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P22	GPIO	00H	00H	●	●	●
	ANI2	00H	00H	●	●	●
	PGA0IN	00H	00H	●	●	●
	PGA1O	00H	00H	●	●	-
	VCIN0	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P23	GPIO	00H	00H	●	●	●
	ANI3	00H	00H	●	●	●
	PGA0GND	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P24	GPIO	00H	00H	●	●	-
	ANI4	00H	00H	●	●	-
	PGA1IN	00H	00H	●	●	-
	PGA0O	00H	00H	●	●	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-
P25	GPIO	00H	00H	●	●	-
	ANI5	00H	00H	●	●	-
	PGA1GND	00H	00H	●	●	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-
P26	GPIO	00H	00H	●	-	-
	ANI6	00H	00H	●	-	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-
P27	GPIO	00H	00H	●	-	-
	ANI7	00H	00H	●	-	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-
P30	GPIO	00H	00H	●	●	●
	ANI21	00H	00H	●	●	●
	INTP3	00H	00H	●	●	●
	RTC1HZ	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●

P31	GPIO	00H	00H	●	●	●
	ANI22	00H	00H	●	●	●
	TI03	00H	00H	●	●	●
	TO03	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P40	GPIO	00H	00H	●	●	●
	SWDIO	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P41	GPIO	00H	00H	●	-	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-
P50	GPIO	00H	00H	●	●	●
	ANI23	00H	00H	●	●	●
	INTP1	00H	00H	●	●	●
	VCOUT1	00H	00H	●	●	●
	(SPINSS)	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P51	GPIO	00H	00H	●	●	●
	ANI24	00H	00H	●	●	●
	INTP2	00H	00H	●	●	●
	(SPISCK)	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P60	GPIO	00H	00H	●	●	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-
P61	GPIO	00H	00H	●	●	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-
P62	GPIO	00H	00H	●	-	-
	ANI27	00H	00H	●	-	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-
P63	GPIO	00H	00H	●	-	-
	ANI28	00H	00H	●	-	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-
P70	GPIO	00H	00H	●	●	●
	ANI29	00H	00H	●	●	●

	KR0	00H	00H	●	●	-
	SCLK21	00H	00H	●	-	-
	SCL21	00H	00H	●	-	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P71	GPIO	00H	00H	●	-	-
	ANI30	00H	00H	●	-	-
	KR1	00H	00H	●	-	-
	SDI21	00H	00H	●	-	-
	SDA21	00H	00H	●	-	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-
P72	GPIO	00H	00H	●	●	●
	ANI31	00H	00H	●	●	●
	KR2	00H	00H	●	●	-
	SDO21	00H	00H	●	-	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P73	GPIO	00H	00H	●	●	●
	ANI32	00H	00H	●	●	●
	KR3	00H	00H	●	●	-
	SDO01	00H	00H	●	●	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P74	GPIO	00H	00H	●	●	●
	ANI33	00H	00H	●	●	●
	KR4	00H	00H	●	●	-
	SDI01	00H	00H	●	●	-
	SDA01	00H	00H	●	●	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P75	GPIO	00H	00H	●	●	-
	ANI34	00H	00H	●	●	-
	KR5	00H	00H	●	●	-
	SCLK01	00H	00H	●	●	-
	SCL01	00H	00H	●	●	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-
P120	GPIO	00H	00H	●	●	●
	ANI14	00H	00H	●	●	●
	VCOUT0	00H	00H	●	●	●

	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P121	GPIO	00H	00H	●	●	●
	X1	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P122	GPIO	00H	00H	●	●	●
	X2	00H	00H	●	●	●
	EXCLK	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P123	GPIO	00H	00H	●	●	-
	XT1	00H	00H	●	●	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-
P124	GPIO	00H	00H	●	●	-
	XT2	00H	00H	●	●	-
	EXCLKS	00H	00H	●	●	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-
P130	GPIO	00H	00H	●	-	-
	ANI35	00H	00H	●	-	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-
P136	GPIO	00H	00H	●	●	●
	ANI36	00H	00H	●	●	●
	INTP0	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P137	GPIO	00H	00H	●	●	●
	SWCLK	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
P140	GPIO	00H	00H	●	●	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	-
P146	GPIO	00H	00H	●	-	-
	ANI15	00H	00H	●	-	-
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	-	-
P147	GPIO	00H	00H	●	●	●
	ANI12	00H	00H	●	●	●

	VREF0	00H	00H	●	●	●
	Configurable digital functions	X (see table 4.1.2)	X (see table 4.1.2)	●	●	●
VDD	Supply voltage	-	-	●	●	●
VSS	Ground	-	-	●	●	●

Table 4.1.2 Digital Function Configuration List (1/2 Output Function Configuration)

Pin name	Control register	Register configuration	Pin alternate function
P00~P147	P00cfg[3:0]~P147cfg[3:0]	4'h00	Default alternate output
		4'h01	TO10
		4'h02	TO11
		4'h03	TO12
		4'h04	TO13
		4'h05	SDO00/TxD0
		4'h06	SDO20/TxD2
		4'h07	CLKBUZ0
		4'h08	SCLKO00
		4'h09	SCLKO20
		4'h0a	TxD1

Note: P60 and P61 are NOD outputs; please pay attention to the configuration when using them.

Table 4.1.2 Digital Function Configuration List (2/2 Input Function Configuration)

Control register	Register configuration	Pin alternate function
TI10PCFG	6'h00	Default alternate input
TI11PCFG	6'h01	P00 as an alternate input
TI12PCFG	6'h02	P01 as an alternate input
TI13PCFG	6'h03	P10 as an alternate input
INTP0PCFG	6'h04	P11 as an alternate input
INTP1PCFG	6'h05	P12 as an alternate input
INTP2PCFG	6'h06	P13 as an alternate input
INTP3PCFG	6'h07	P14 as an alternate input
SDI00PCFG (SPI/IIC/UART)	6'h08	P15 as an alternate input
SCLKI00PCFG (SPI/IIC)	6'h09	P16 as an alternate input
SS00PCFG (SPI)	6'h0a	P17 as an alternate input
SDI20PCFG (SPI/UART)	6'h0b	P20 as an alternate input
SCLKI20PCFG (SPI)	6'h0c	P21 as an alternate input
RXD1PCFG (UART)	6'h0d	P22 as an alternate input
SDAA0PCFG	6'h0e	P23 as an alternate input
SCLA0PCFG	6'h0f	P24 as an alternate input
	6'h10	P25 as an alternate input
	6'h11	P26 as an alternate input
	6'h12	P27 as an alternate input
	6'h13	P30 as an alternate input
	6'h14	P31 as an alternate input
	6'h15	P40 as an alternate input
	6'h16	P41 as an alternate input
	6'h17	P50 as an alternate input
	6'h18	P51 as an alternate input

	6’h19	P60 as an alternate input
	6’h1a	P61 as an alternate input
	6’h1b	P62 as an alternate input
	6’h1c	P63 as an alternate input
	6’h1d	P70 as an alternate input
	6’h1e	P71 as an alternate input
	6’h1f	P72 as an alternate input
	6’h20	P73 as an alternate input
	6’h21	P74 as an alternate input
	6’h22	P75 as an alternate input
	6’h23	P120 as an alternate input
	6’h24	P121 as an alternate input
	6’h25	P122 as an alternate input
	6’h26	P123 as an alternate input
	6’h27	P124 as an alternate input
	6’h28	P130 as an alternate input
	6’h29	P136 as an alternate input
	6’h2a	P137 as an alternate input
	6’h2b	P140 as an alternate input
	6’h2c	P146 as an alternate input
	6’h2d	P147 as an alternate input

Table 4.1.3 SPI Pin Function Configuration List

Register name	Register setting	SPI pin function mapping			
		SPINSS	SPISCK	SPIMISO	SPIMOSI
SPIPCFG[1:0]	2’b00	Not mapped to any pin			
	2’b01	P50	P51	P17	P16
	2’b10	P63	P31	P75	P74
	1’b11	P25	P24	P23	P22

4.2 Port Alternate Functions

(1/2)

Function name	Input/Output	Function
ANI0 ~ANI36	Input	A/D converter analog input
INTP0 ~INTP3	Input	External interrupt request input Specification of active edges: rising edge, falling edge, rising and falling edges
VCIN0	Input	Comparator 0 analog voltage input
VCIN10, VCIN11, VCIN12, VCIN13	Input	Comparator 1 analog voltage / reference voltage input
VREF0	Input	Comparator 0 reference voltage input
VCOUT0, VCOUT1	Output	Comparator output
PGA0IN, PGA1IN	Input	PGA input
PGA0O, PGA1O	Output	PGA output
PGA0GND, PGA1GND	Input	PGA reference input
KR0 ~KR5	Input	Key interrupt input
CLKBUZ0, CLKBUZ1	Output	Clock output / Buzzer output
RTC1HZ	Output	Real-time clock correction clock (1Hz) output
RESETB	Input	Low-level active system reset input, when external reset is not used, it must be connected directly or through a resistor to VDD.
IrRxD	Input	IrDA serial data input
IrTxD	Output	IrDA serial data output
RxD0 ~RxD2	Input	Serial data inputs of serial interfaces UART0, UART1, UART2
TxD0 ~TxD2	Output	Serial data outputs of serial interfaces UART0, UART1, UART2
SCL00, SCL01, SCL10, SCL11, SCL20, SCL21	Output	Serial clock outputs of serial interfaces IIC00, IIC01, IIC10, IIC11, IIC20, IIC21
SDA00, SDA01, SDA10, SDA11, SDA20, SDA21	Input/Output	Serial data inputs/outputs of serial interfaces IIC00, IIC01, IIC10, IIC11, IIC20, IIC21
SCLK00, SCLK01, SCLK10, SCLK11, SCLK20, SCLK21	Input/Output	Serial clock inputs/outputs of serial interfaces SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21
SDI00, SDI01, SDI10, SDI11, SDI20, SDI21	Input	Serial data inputs of serial interfaces SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21

(2/2)

Function name	Input/Output	Function
SS00	Input	Serial interface SSPI00 chip select input
SDO00, SDO01, SDO10, SDO11, SDO20, SDO21	Output	Serial data outputs of SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21
SPINSS	Input	Serial interface SPI chip select input
SPISCK	Input/Output	Serial interface SPI serial clock input/output
SPIMISO	Input/Output	Serial interface SPI serial data input/output
SPIMOSI	Input/Output	Serial interface SPI serial data input/output
SCLA0	Input/Output	Serial interface IICA0 clock input/output
SDAA0	Input/Output	Serial interface IICA0 serial data input/output
TI00~TI03	Input	External counting clock / capture trigger input for 16-bit Timer40
TO00~TO03	Output	Timer output for 16-bit Timer40
TI10~TI13	Input	External counting clock / capture trigger input for 16-bit Timer41
TO10~TO13	Output	Timer output for 16-bit Timer41
X1, X2	—	Resonator for the main system clock connection
EXCLK	Input	External clock input for the main system clock
XT1, XT2	—	Resonator for the sub-system clock connection
EXCLKS	Input	External clock input for the sub-system clock
VDD	—	Power supply
AVREFP	Input	Positive (+) reference voltage input for the A/D converter
AVREFM	Input	Negative (–) reference voltage input for the A/D converter
VSS	—	Ground
SWDIO	Input/Output	SWD data interface
SWCLK	Input	SWD clock interface

Note: As a countermeasure against noise and locking, a bypass capacitor (around 0.1μF) must be connected between VDD and VSS with the shortest possible distance and using thicker traces.

5 Function Summary

5.1 ARM® Cortex®-M0+ Core

The ARM Cortex-M0(+) processor is a next-generation product in the ARM processor family, designed specifically for embedded systems. It provides a low-cost platform aimed at meeting the needs of microcontrollers with a small pin count and low power consumption, while delivering excellent computational performance and advanced system response to interrupts.

The Cortex-M0(+) processor is a 32-bit RISC processor, offering superior code efficiency and delivering the high-performance expectations of the ARM core, distinguishing itself from 8-bit and 16-bit devices of the same memory size. The Cortex-M0(+) processor features 32 address lines, with a memory space of up to 4GB.

The BAT32G135B integrates an embedded ARM core, making it fully compatible with all ARM tools and software.

5.2 Memory

5.2.1 Flash Memory

The BAT32G135B features an internal flash memory that is programmable, erasable, and rewriteable. It includes the following functionalities:

- 64K program memory space.
- 1.5KB dedicated data flash memory.
- Supports page erase, with each page size of 512 bytes and an erase time of 4ms.
- Supports byte/half-word/word (32-bit) programming, with a programming time of 24μs.

5.2.2 SRAM

The BAT32G135B features 8KB of embedded SRAM

5.3Enhanced DMA Controller

The BAT32G135B is equipped with an enhanced DMA (Direct Memory Access) controller, enabling data transfer between memory regions without using the CPU.

- It supports triggering DMA via peripheral function interrupts, allowing real-time control through communication, timers, and A/D conversions.
- The source and target fields for transfer can be selected from the entire address space (when the flash is used as the target address, it must be preset to programming mode).
- It supports four transfer modes: normal transfer mode, repeat transfer mode, block transfer mode, and chain transfer mode.

5.4Linkage Controller

The linkage controller connects events generated by various peripheral functions with their triggering sources, enabling direct collaboration between peripheral functions without involving the CPU.

The linkage controller includes the following features:

- It can link event signals together to realize the linkage of peripheral functions.
- It supports 15 types of event inputs and 4 types of event triggers.

5.5 Clock Generation and Startup

The clock generation circuit is responsible for providing clock signals to the CPU and peripheral hardware. There are three types of system clocks and clock oscillation circuits:

5.5.1 Main System Clock

- X1 Oscillator Circuit: This circuit can generate a clock oscillation ranging from 1 to 20 MHz by connecting a resonator to the X1 and X2 pins. The oscillation can be stopped by executing the deep sleep instruction or setting the MSTOP bit.
- High-Speed On-Chip Oscillator (High-Speed OCO): The frequency of oscillation can be selected through an option byte. After a reset is released, the CPU defaults to running with this high-speed on-chip oscillator clock. The oscillation can be stopped by executing the deep sleep instruction or setting the HIOSTOP bit. The frequency set by the option byte can be changed using the frequency selection register of the high-speed on-chip oscillator. The maximum frequency is 64 MHz, with an accuracy of ±1.0%.
- External Clock Input via Pin (X2): The external clock input (1~20 MHz) can be provided through the X2 pin. The input can be disabled by executing the deep sleep instruction or setting the MSTOP bit.
- PLL Phase-Locked Loop Circuit: The PLL circuit multiplies the frequency of the X1 oscillator or the high-speed on-chip oscillator circuit to provide a system clock of up to 64 MHz. The PLL oscillation and stop functions are controlled by the PLL control register (PLLCR).

5.5.2 Subsystem Clock

- XT1 Oscillator Circuit: This circuit can generate a 32.768 kHz clock oscillation by connecting a 32.768 kHz resonator to the XT1 and XT2 pins. The oscillation can be stopped by setting the XTSTOP bit.
- External Clock Input via Pin (XT2): An external 32.768 kHz clock can be provided through the XT2 pin. The input can be disabled by setting the XTSTOP bit.

5.5.3 Low-Speed On-chip Oscillator Clock

- Low-Speed On-Chip Oscillator (Low-Speed OCO): This oscillator generates a clock oscillation of 15 kHz (typical value). The low-speed on-chip oscillator clock can be used as the CPU clock. The following peripheral hardware can also operate using the low-speed on-chip oscillator clock:
- Watchdog Timer (WWDT)
- Real-Time Clock (RTC)
- 15-bit Interval Timer

5.6 Power Management

5.6.1 Power Supply Mode

VDD: External power supply, with a voltage range of 1.8 to 5.5V.

5.6.2 Power-On Reset

The Power-on Reset (POR) circuit has the following functions:

- It generates an internal reset signal when the power is turned on. The reset is released when the supply voltage (V_{DD}) exceeds the detection voltage (V_{POR}). However, before the operating voltage range is reached, the reset state must be maintained through a voltage detection circuit or external reset.
- It compares the supply voltage (V_{DD}) with the detection voltage (V_{PDR}). When $V_{DD} < V_{PDR}$, an internal reset signal is generated. However, during a power-down event, before the voltage falls below the operating voltage range, the system must transition to deep sleep mode or be reset through a voltage detection circuit or external reset. To resume operation, it must be ensured that the supply voltage has returned to the operating voltage range.

5.6.3 Voltage Detection

The voltage detection circuit sets the operating mode and detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) through the option byte. The Low Voltage Detection (LVD) circuit has the following functions:

- It compares the supply voltage (V_{DD}) with the detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) and generates an internal reset or interrupt request signal.
- The detection voltage (V_{LVDH}, V_{LVDL}, V_{LVD}) for the supply voltage can be selected through the option byte.
- It can operate in deep sleep mode.
- When the supply voltage rises, the reset state must be maintained through the voltage detection circuit or external reset until the operating voltage range is reached. When the supply voltage drops, the system must transition to deep sleep mode or be reset through the voltage detection circuit or external reset before it falls below the operating voltage range.
- The operating voltage range is determined by the settings of the user option byte.

5.7 Low Power Modes

The BAT32G135B supports two low-power modes to achieve the best compromise between low power consumption, short startup time, and available wakeup sources:

- Sleep Mode: Sleep mode is entered by executing the sleep instruction. In this mode, the CPU clock is stopped, but if the high-speed system clock oscillator, high-speed on-chip oscillator, or sub-system clock oscillator is oscillating, these clocks continue to oscillate. While this mode does not reduce the operating current as much as deep sleep mode, it is an effective mode when immediate reprocessing is needed via interrupt requests or when intermittent operation is required.
- Deep Sleep Mode: Deep sleep mode is entered by executing the deep sleep instruction. In this mode, the high-speed system clock oscillator and high-speed on-chip oscillator are stopped, and the entire system is in a low-power state. This significantly reduces the chip's operating current. Since deep sleep mode can be released through interrupt requests, it also allows for intermittent operation. However, in the case of the X1 clock, the oscillation stability waiting time must be ensured when releasing deep sleep mode. Therefore, if immediate processing via an interrupt request is required, sleep mode should be selected.

In both modes, registers, flags, and data memory retain their values as they were before entering the standby mode, and the states of input/output port output latches and output buffers are also maintained.

5.8 Reset Function

There are 7 methods to generate a reset signal:

1) A reset signal is generated by inputting an external reset through the RESETB pin.
2) A reset signal is generated internally when the watchdog timer detects a program failure.
3) A reset signal is generated by comparing the power voltage with the detection voltage from the Power-On Reset (POR) circuit.
4) A reset signal is generated by comparing the power voltage with the detection voltage from the Low Voltage Detection (LVD) circuit.
5) A reset signal is generated when a parity error occurs in RAM.
6) A reset signal is generated when illegal memory access occurs.
7) A reset signal generated by software.

Both internal and external resets behave the same way. After the reset signal is generated, program execution starts from the address written in addresses 0000H and 0001H.

5.9 Interrupt Function

The Cortex-M0+ processor integrates a Nested Vectored Interrupt Controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs and 1 non-maskable interrupt (NMI) input. In addition, the processor supports several internal exceptions.

This product handles 32 maskable IRQs and 1 NMI, as detailed in the corresponding section of the user manual. The actual number of interrupt sources may vary depending on the specific product.

5.10 Real-Time Clock (RTC)

Functions of real-time clock (RTC) are show as below.

- Holds counters for years, months, weeks, days, hours, minutes, and seconds
- Fixed cycle break (cycles: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm clock interrupt (alarm clock: week, hour, minute)
- 1Hz pin out capability
- Support prescalers of subsystem clock or main system clock as RTC operation clocks.
- Real-time clock interrupt signals (INTRTC) can be used to wake up in deep sleep mode.
- Clock error correction with wide range

Year, month, week, day, hour, minute and second counters are only available if the subsystem clock (32.768kHz) or main system clock prescaler is selected as the RTC operation clock. When the low-speed on-chip oscillator clock (15kHz) is selected, only the fixed-cycle interrupt function can be used.

5.11 Watchdog Timer

The 1- channel WWDT and 17-bit watchdog timer operations are set by option bytes. The watchdog timer operates on a low-speed on-chip oscillator clock (15KHz). The watchdog timer is used to detect program failure. When program failure is detected, an internal reset signal is generated.

The following situations are considered as program failure detection:

- When the watchdog timer counter overflows.
- When a 1-bit operation instruction is executed on the watchdog timer enable register (WDTE).
- When data other than “ACH” is written to the WDTE register.
- When data is written to the WDTE register during the window closed period.

5.12 SysTick Timer

This timer is dedicated to real-time operating systems, but can also be used as a standard decrementing counter.

Its features include: A 24-bit decrementing counter with auto-reload capability. When the counter reaches 0, a maskable system interrupt is generated.

5.13 Timer4

This product features 2 timer units, each containing 4 channels of 16-bit timers, referred to as Timer4. Each 16-bit timer is called a “channel” and can be used either as an independent timer or combined with other channels to perform advanced timer functions.

For detailed information on each function, please refer to the table below.

Independent channel operation function	Multi-channel linkage operation function
● Interval timer ● Square wave output ● External event counter ● Frequency divider ● Input pulse interval measurement ● Input signal high/low width measurement ● Delay counter	● Single trigger pulse output ● PWM output ● Multiple PWM output

5.13.1 Independent Channel Operation Function

The independent channel operation function allows a channel to operate independently without being influenced by the operation mode of other channels. This function can be used in the following modes:

1) Interval Timer: Used as a reference timer to generate interrupts (INTTM) at fixed intervals.
2) Square Wave Output: Each time an INTTM interrupt occurs, a toggle is triggered, and a 50% duty cycle square wave is output from the timer output pin (TO).
3) External Event Counter: Counts the valid edges of the input signal on the timer input pin (TI). When the count reaches a specified value, it can be used as an event counter to generate an interrupt.
4) Frequency Divider Function (Limited to Unit 0, Channel 0): Divides the input clock signal at the timer input pin (TI00) and then outputs the divided signal from the output pin (TO00).
5) Input Pulse Interval Measurement: Starts counting on the valid edge of the input pulse signal on the timer input pin (TI), and captures the counter value on the next valid edge of the pulse, thereby measuring the input pulse interval.
6) Input Signal High/Low Level Width Measurement: Starts counting on one edge of the input signal at the timer input pin (TI) and captures the counter value at the other edge, thereby measuring the high or low level width of the input signal.
7) Delay Counter: Starts counting on the valid edge of the input signal on the timer input pin (TI), and generates an interrupt after a specified delay.

5.13.2 Multi-Channel Linked Operation Function

The multi-channel linked operation function allows the combination of a master channel (the reference timer controlling the main cycle) and slave channels (timers that follow the master channel's operation). This function can be used in the following modes:

1) Single-Trigger Pulse Output: Two channels are used in pairs to generate single-trigger pulses with adjustable output timing and pulse width.
2) PWM (Pulse Width Modulation) Output: Two channels are used in pairs to generate pulses with adjustable periods and duty cycles.
3) Multiple PWM (Pulse Width Modulation) Output: Expands the PWM function and uses one master channel with multiple slave channels to generate up to 3+3 types of PWM signals with arbitrary duty cycles, all with a fixed period.

5.13.3 8-Bit Timer Operation Function

The 8-bit timer operation function allows a 16-bit timer channel to be used as two 8-bit timer channels. (Only channel 1 and channel 3 can be used for this function.)

5.13.4 LIN-Bus Support Function

The Timer4 unit can be used to check if the received signal in the LIN-bus communication matches the LIN-bus communication format.

1) Wake-up Signal Detection: Counting starts on the falling edge of the input signal on the UART serial data input pin (RxD), and the count value is captured on the rising edge, measuring the low-level width. If the low-level width is greater than or equal to a specified value, it is considered a wake-up signal.
2) Break Field Detection: After detecting the wake-up signal, counting starts on the falling edge of the input signal on the UART serial data input pin (RxD), and the count value is captured on the rising edge to measure the low-level width. If the low-level width is greater than or equal to a specified value, it is considered a break field.
3) Synchronization Field Pulse Width Measurement: After detecting the break field, the low-level and high-level pulse widths of the input signal on the UART serial data input pin (RxD) are measured. The bit interval of the synchronization field is used to calculate the baud rate.

5.14 EPWM Output Control Circuit

By using the Timer4 PWM output function, control of a DC motor or two stepper motors can be achieved. The output can be interrupted by truncating the source CMP0 output, INTP0 input, and EVENTC event. Through software settings, four types of outputs can be selected from forced truncation: Hi-Z output, low-level output, high-level output, and disabling output truncation.

5.15 15-Bit Interval Timer

This product includes a built-in 15-bit interval timer that can generate interrupts (INTIT) at any pre-set time interval. It can be used to wake up from deep sleep mode.

5.16 Clock Output/Buzzer Output Controller

The clock output controller is used to provide a clock signal to external ICs, while the buzzer output controller generates a square wave for the buzzer frequency. The clock output or buzzer output is implemented through dedicated pins.

5.17 Universal Serial Communication Unit

This product is equipped with two Universal Serial Communication Units. Unit 0 has four serial communication channels, and Unit 1 has two serial communication channels. It supports communication functions for standard SPI, simplified SPI, UART, and simplified I2C. The functionality allocation for each channel is as follows:

5.17.1 3-Wire Serial Interface (Simplified SPI)

Data transmission and reception are synchronized with the serial clock (SCK) output by the master device.

This interface uses 3 communication lines: 1 serial clock (SCK), 1 transmit serial data (SO), and 1 receive serial data (SI).

[Data transmission and reception]

- Data length of 7 or 8 bits
- Phase control of data transmission and reception
- MSB/LSB first

[Clock control]

- Master or slave selection
- Phase control of input/output clock
- Transfer cycles generated by prescalers and channel internal counters
- Maximum transfer rate

Master communication: Max. $F_{CLK}/2$

Slave communication: Max. $F_{MCK}/6$

[Interrupt function]

- Transfer end interrupt, buffer null interrupt

[Error detection flags]

- Overflow errors

5.17.2 Simplified SPI with Slave Chip Select Function

This interface supports SPI serial communication with a slave chip select input function. It uses four communication lines: 1 slave chip select input (SSI), 1 serial clock (SCK), 1 transmit serial data (SO), and 1 receive serial data (SI), for clock-synchronized communication.

[Data transmission and reception]

- Data length of 7 or 8 bits
- Phase control of data transmission and reception
- MSB/LSB first
- Level settings of transmit and receive data

[Clock control]

- Phase control of input/output clocks
- Transfer cycles generated by prescalers and channel internal counters
- Maximum transfer rate

Slave communication: Max.f_{MCK}/6

[Interrupt function]

- Transfer end interrupt, buffer null interrupt

[Error detection flags]

- Overflow errors

5.17.3 UART

The function enables asynchronous communication using two lines: Serial Data Transmission (TxD) and Serial Data Reception (RxD). With these two communication lines, data is transmitted and received asynchronously (using an internal baud rate) according to a data frame structure consisting of a start bit, data, parity bit, and stop bit. Full-duplex UART communication can be achieved by using two dedicated channels: one for transmission (even channel) and one for reception (odd channel). Additionally, by combining Timer 4 and external interrupt (INTP0), it supports LIN-bus communication.

[Data transmission and reception]

- Data length of 7, 8, or 9 bits
- MSB/LSB first
- Level setting for transmitting and receiving data, selection of inversion
- Parity bit appending, parity check function
- Stop bit appending, stop bit detection

[Interrupt function]

- Transfer end interrupt, buffer null interrupt
- Error interrupts caused by frame errors, parity check errors, or overflow errors

[Error detection flags]

- Frame errors, parity errors, overflow errors

[LIN-bus function]

- Detection of wake-up signals
- Detection of break fields (BF)
- Measurement of synchronous fields, calculation of baud rate

5.17.4 Simplified I^2C

The function enables clock-synchronized communication with multiple devices using two lines: Serial Clock (SCL) and Serial Data (SDA). This simplified I^2C is designed for single-device communication with peripherals such as flash memory, A/D converters, and similar devices, and thus can only be used as the master device. The start and stop conditions, along with the operation control register, must adhere to the AC characteristics and are processed through software.

[Data transmission and reception]

- Master transmission, master reception (limited to the master function of single master)
- ACK output function [Note], ACK detection function
- 8-bit data length (when transmitting the addresses, specify the addresses with the higher 7 bits, and use the lowest bit for R/W control)
- Start and stop conditions are generated by software

[Interrupt function]

- Transfer end interrupt

[Error detection flags]

- ACK errors, overflow errors

[Simplified I^2C unsupported features]

- Slave transmission, slave reception
- Multi-master function (arbitration failure detection function)
- Wait detection function

5.18 Standard Serial Interface (SPI)

The Serial Peripheral Interface (SPI) has the following two modes:

- Run Stop Mode: This mode is used when no serial transfer is taking place, helping to reduce power consumption.
- 3-wire Serial I/O Mode: In this mode, data transfer occurs with multiple devices using three lines: Serial Clock (SCK) and Serial Data Lines (MISO and MOSI), supporting 8-bit or 16-bit data transfer.

5.19 Standard Serial Interface (IICA)

The Serial Interface IICA has the following three modes:

- Run Stop Mode: This mode is used when no serial transfer is taking place, helping to reduce power consumption.
- I2C Bus Mode (Supports Multiple Masters): In this mode, communication with multiple devices is achieved using two lines: Serial Clock (SCLA) and Serial Data Bus (SDAA), for 8-bit data transfer. It follows the I2C bus protocol, where the master device generates the “start condition”, “address”, “transfer direction indication”, “data”, and “stop condition” on the serial data bus. The slave devices automatically detect the received status and data through hardware. This functionality simplifies the I2C bus control part of the application. Since the SCLA and SDAA pins of the Serial Interface IICA are open-drain outputs, the serial clock line and serial data bus require pull-up resistors.
- Wakeup Mode: In deep sleep mode, when an extended code or local station address is received from the master device, it can wake up the system by generating an interrupt request signal (INTIICA) to exit deep sleep mode. This is configurable via the IICA control register.

5.20 Analog-to-Digital Converter (ADC)

This product includes a 12-bit SAR (Successive Approximation Register) ADC that converts analog inputs into digital values, supporting up to 35 ADC analog input channels (ANI0~ANI24, ANI27~ANI36). The ADC has the following features:

- 12-bit Resolution, conversion rate of 1.42 Msps.
- Trigger Modes: Supports software trigger, hardware trigger, and hardware trigger in standby mode.
- Channel Selection: Supports both single-channel selection and multi-channel scanning modes.
- Conversion Modes: Supports single conversion and continuous conversion modes.
- Operating Voltage: Supports an operating voltage range of 1.8V ≤ VDD ≤ 5.5V.
- Internal Voltage Reference and Temperature Sensor: Can detect the built-in reference voltage (1.45V) and the temperature sensor.

The ADC can be configured into various A/D conversion modes through combinations of the modes mentioned below.

Trigger mode	Software trigger	Start the conversion by operating the software.
	Hardware-trigger no-wait mode	The conversion is started by detecting a hardware trigger.
	Hardware trigger wait mode	In the conversion standby state when the power is cut off, the power is turned on by detecting the hardware trigger, and the conversion starts automatically after the A/D power stabilization waiting time.
Channel select mode	Select mode	Select 1 channel of analog input for A/D conversion.
	Scan mode	Four consecutive channels from ANI0 to ANI15 can be selected as analog inputs for sequential A/D conversion.
Conversion mode	Single conversion mode	Perform an A/D conversion for the selected channel.
	Continuous conversion mode	Perform continuous A/D conversions for the selected channel until stopped by the software.
Sample time/conversion time	Number of sample clocks/ conversion clocks	The sampling time can be set by a register, the default value of sampling clock number is 13.5 clk, and the minimum value of conversion clock number is 31.5 clk.

5.21 Programmable Gain Amplifier (PGA)

This product includes two built-in programmable gain amplifiers (PGA0 and PGA1) with the following features:

- Each PGA has 7 selectable gain options: 4x, 8x, 10x, 12x, 14x, 16x, and 32x.
- An external pin can be selected as the ground for the PGA negative feedback resistor .
- The output of PGA0 can be selected as the analog input for the A/D converter or the positive input for Comparator 0 (CMP0).
- The output of PGA1 can be selected as the analog input for the A/D converter.

5.22 Comparator (CMP)

This product includes two built-in comparators, CMP0 and CMP1, with the following features:

- Supports selection of comparator high-speed mode, low-speed mode, or comparator window mode.
- Allows selection of an external reference voltage input or internal reference voltage for the reference voltage.
- Supports selection of the noise elimination digital filter width.
- Can detect the valid edge of the comparator output and generate an interrupt signal.
- Can detect the valid edge of the comparator output and output the event signal to the linked controller.

5.23 Two-Wire Serial Debug Port (SW-DP)

The ARM SW-DP interface allows the connection of a serial debugging tool to the microcontroller.

5.24 Safety Functions

5.24.1 Flash Memory CRC Calculation Function (High-Speed CRC, Universal CRC)

This function detects data errors in the flash memory through CRC calculations.
Depending on the usage and conditions, two types of CRC can be used:

- High-Speed CRC: Stops CPU operation during initialization to perform high-speed checks on the entire code flash area.
- Universal CRC: Can be used during CPU operation for multi-purpose checks, not limited to the code flash area.

5.24.2 RAM Parity Error Detection Function

Detects parity errors when reading RAM data.

5.24.3 SFR Protection Function

Prevents the overwriting of important Special Function Registers (SFR) due to CPU malfunction.

5.24.4 Illegal Memory Access Detection Function

Detects illegal access to memory areas that are either non-existent or access-restricted.

5.24.5 Frequency Detection Function

Uses the Timer 4 unit to self-detect the CPU or peripheral hardware clock frequency.

5.24.6 A/D Test Function

Performs self-testing of the A/D converter by converting the positive (+) and negative (–) reference voltages, analog input channels (ANI), temperature sensor output voltage, and internal reference voltage.

5.24.7 Digital Output Signal Level Detection Function for I/O Ports

When the I/O port is set to output mode, the output level of the pin can be read.

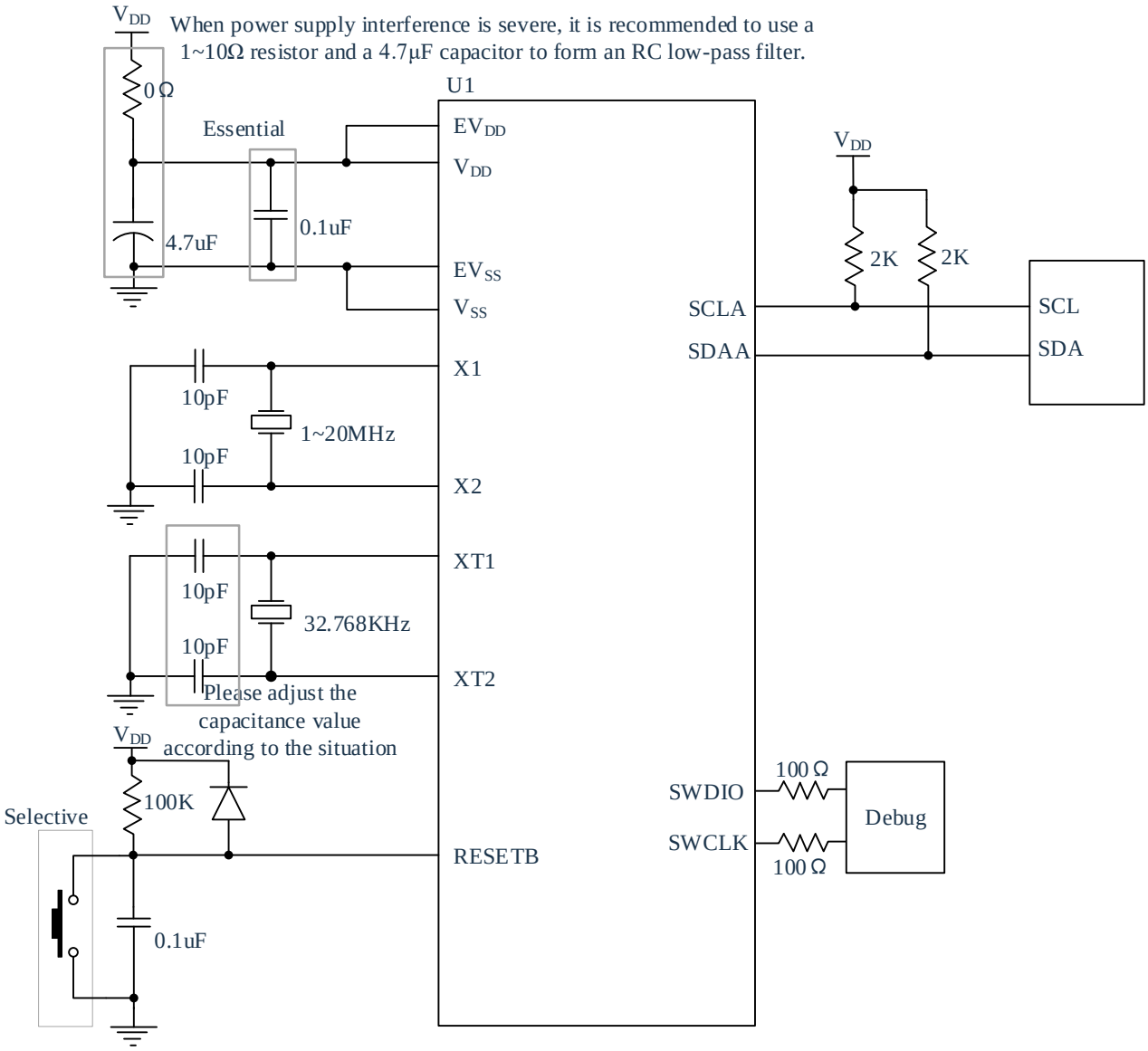
5.25 Key Function

A key interrupt (INTKR) can be generated by inputting the falling edge of the key interrupt input pins (KR0~KR4).

6 Electrical Characteristics

6.1 Typical Application Peripheral Circuit

The device connection reference diagram for the typical MCU application peripheral circuit is as follows:



6.2 Absolute Maximum Voltage Ratings

(T_A=–40~+105℃)

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.5~+6.5	V
Input voltage	V_{I1}	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41, P50~P51, P62~P63, P70~P75, P120~P124, P130, P136, P137, P140, P146, P147, EXCLK, EXCLKS, RESETB	–0.3~V_{DD}+0.3 Note 1	V
	V_{I2}	P60~P61 (N-channel open drain)	–0.3~+6.5	V
Output voltage	V_O	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41, P50~P51, P60~P63, P70~P75, P120, P130, P136, P137, P140, P146, P147	–0.3~V_{DD}+0.3 Note 1	V
Analog input voltage	V_{AI}	ANI0~ANI24, ANI27~ANI36	–0.3~V_{DD}+0.3 and –0.3~AV_{REF}(+)+0.3 Note 1, 2	V

Note 1: Not more than 6.5V.

Note 2: The pin of the A/D conversion target cannot exceed AV_{REF} (+)+0.3.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks:

1. Unless otherwise specified, the characteristics of alternated pins are the same as those of port pins.
2. AV_{REF}(+): A/D converter positive (+) reference voltage
3. Set V_{SS} as the reference voltage

6.3 Absolute Maximum Current Ratings

(T_A=–40~+105℃)

Item	Symbol	Condition		Rating	Unit
Output current, high	I_{OH1}	Per pin	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41, P50~P51, P62~P63, P70~P75, P120, P130, P136, P137, P140, P146, P147	-40	mA
		Total of all pins –170mA	P00~P01, P20~P27, P40~P41, P120, P130, P136, P137, P140	-70	mA
			P10~P17, P30~P31, P50~P51, P62~P63, P70~P75, P146, P147	-100	mA
	I_{OH2}	Per pin	P121~P124	-3	mA
		Total of all pins		-15	mA
Output current, low	I_{OL1}	Per pin	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41, P50~P51, P60~P63, P70~P75, P120, P130, P136, P137, P140, P146, P147	40	mA
		Total of all pins 170mA	P00~P01, P20~P27, P40~P41, P120, P130, P136, P137, P140	100	mA
			P10~P17, P30~P31, P50~P51, P60~P63, P70~P75, P146, P147	120	mA
	I_{OL2}	Per pin	P121~P124	15	mA
		Total of all pins		45	mA
Operating ambient temperature	T_A	In normal operation mode		-40~+105	℃
		In flash memory programming mode			
Storage temperature	T_{stg}	-		-65~ +150	℃

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark: Unless otherwise specified, the characteristics of alternated pins are the same as those of port pins.

6.4 Oscillation Circuit Characteristics

6.4.1 X1 and XT1 Characteristics

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Resonator	Condition	Min.	Typ.	Max.	Unit
X1 clock oscillation frequency (f_X)	Ceramic/crystal resonator		1.0	-	20.0	MHz
X1 clock oscillation stabilization time	Ceramic/crystal resonator	20MHz, C=10pF		15		mS
X1 clock oscillation feedback resistor	Ceramic/crystal resonator		0.6		1.8	MΩ
XT1 clock oscillation frequency (f_{XT})	Crystal resonator		32	32.768	35	KHz
XT1 clock oscillation stabilization time	Crystal resonator	32.768KHz, C=10pF		2		S

Remarks:

1. It only indicates the frequency tolerance range of the oscillation circuit, and the instruction execution time should be referred to the AC characteristics.
2. Please ask the resonator manufacturer to evaluate the circuit after installation, and use it after confirming the oscillation characteristics.

6.4.2 Internal Oscillator Characteristics

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Resonator	Condition	Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency (f_{IH}) Note 1,2		1.0		64.0	MHz
High-speed on-chip oscillator stabilization time (t_{SU})			12		us
High-speed on-chip oscillator clock frequency accuracy	T_A= 10~+70℃	-1.0		+1.0	%
	T_A= -20~+105℃	-2.0 Note 3		+2.0 Note 3	%
	T_A=–40~+105℃	-4.0 Note 3		+4.0 Note 3	%
Low-speed on-chip oscillator clock frequency (f_{IL})		12	15	18	KHz

Note 1: Select the frequency of the high-speed on-chip oscillator via the option byte.

Note 2: It only indicates the characteristics of the oscillation circuit, so please refer to the AC characteristics for the instruction execution time.

Note 3: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.4.3 PLL Oscillator Characteristics

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Resonator	Condition	Min.	Typ.	Max.	Unit
PLL input frequency Note 1	-	4.0	-	8.0	MHz
PLL lock time	-	-	-	20	us

Note 1: It only indicates the characteristics of the oscillation circuit, so please refer to the AC characteristics for the instruction execution time.

Remark: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.5DC Characteristics

6.5.1 Pin Characteristics

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output current, high Note 1	I_{OH1}	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41, P50~P51, P62~P63, P70~P75, P120, P130, P136, P137, P140, P146, P147 Per pin	1.8V≤V_{DD}≤5.5V –40~+85℃			-12.0 Note 2	mA
			1.8V≤V_{DD}≤5.5V 85~+105℃			-6.0 Note 2	
		P00~P01, P20~P27, P40~P41, P120, P130, P136, P137, P140 Total (when duty cycle≤70% Note3)	4.0V≤V_{DD}≤5.5V –40~+85℃			-60.0	mA
			4.0V≤V_{DD}≤5.5V 85~+105℃			-30.0	
			2.4V≤V_{DD}＜4.0V			-12.0	mA
			1.8V≤V_{DD}＜2.4V			-6.0	mA
		P10~P17, P30~P31, P50~P51, P62~P63, P70~P75, P146, P147 Total (when duty cycle≤70% Note3)	4.0V≤V_{DD}≤5.5V –40~+85℃			-80.0	mA
			4.0V≤V_{DD}≤5.5V 85~+105℃			-30.0	
			2.4V≤V_{DD}＜4.0V			-20.0	mA
			1.8V≤V_{DD}＜2.4V			-10.0	mA
		Total (when duty cycle≤70% Note3)	1.8V≤V_{DD}≤5.5V –40~+85℃			-140.0	mA
			1.8V≤V_{DD}≤5.5V 85~+105℃			-60.0	
	I_{OH2}	P121 ~ P124 Per pin	1.8V≤V_{DD}≤5.5V			-2.5 Note 2	mA
		Total (when duty cycle≤70% Note3)	1.8V≤V_{DD}≤5.5V			-10	mA

Note 1: This is the current value that guarantees device operation even if current flows from the V_{DD} pin to the output pin(s).

Note 2: The total current value cannot be exceeded.

Note 3: This is the output current value for the condition “duty cycle≤70%”.

The output current value for a duty cycle > 70% can be calculated using the following equation (in the case of changing the duty cycle to n%).

• Total output current of pins = (I_{OH}×0.7)/(n×0.01)

<Example> I_{OH} =–10.0mA, n =80%

Total output current of pins = (–10.0×0.7)/(80×0.01) ≈ –8.7mA

The current at each pin does not vary by duty cycle and does not flow above the absolute maximum rating.

Remark: Unless otherwise specified, the characteristics of alternated pins are the same as those of port pins.

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output current, low[Note 1]	I_{OL1}	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41, P50~P51, P60~P63, P70~P75, P120, P130, P136, P137, P140, P146, P147 Per pin	1.8V≤V_{DD}≤5.5V –40~+85℃			35[Note 2]	mA
			1.8V≤V_{DD}≤5.5V 85~+105℃			20[Note 2]	
		P00~P01, P20~P27, P40~P41, P120, P130, P136, P137, P140 Total (when duty cycle≤70% [Note3])	4.0V≤V_{DD}≤5.5V –40~+85℃			100	mA
			4.0V≤V_{DD}≤5.5V 85~+105℃			70	
			2.4V≤V_{DD}＜4.0V			30	mA
			1.8V≤V_{DD}＜2.4V			15	mA
		P10~P17, P30~P31, P50~P51, P60~P63, P70~P75, P146, P147 Total (when duty cycle≤70% [Note3])	4.0V≤V_{DD}≤5.5V –40~+85℃			120	mA
			4.0V≤V_{DD}≤5.5V 85~+105℃			80	
			2.4V≤V_{DD}＜4.0V			40	mA
			1.8V≤V_{DD}＜2.4V			20	mA
		Total of all pins (when duty cycle≤70% [Note3])	1.8V≤V_{DD}≤5.5V –40~+85℃			150	mA
			1.8V≤V_{DD}≤5.5V 85~+105℃			100	
	I_{OL2}	P121 ~ P124 per pin	1.8V≤V_{DD}≤5.5V			10[Note 2]	mA
		Total of all pins (when duty cycle≤70% [Note3])	1.8V≤V_{DD}≤5.5V			40	mA

Note 1: This is the current value guarantees device operation if current flows from the output pin(s) to the V_{SS} pin.

Note 2: The total current value cannot be exceeded.

Note 3: This is the output current value for the condition “duty cycle≤70%”.

The output current value for a duty cycle > 70% can be calculated using the following equation (in the case of changing the duty cycle to n%).

• Total output current of pins = (I_{OL}×0.7)/(n×0.01)

<Example> I_{OL}= 10.0mA, n = 80%

Total output current of pins = (10.0×0.7)/(80×0.01) ≈ 8.7mA

The current at each pin does not vary by duty cycle and does not flow above the absolute maximum rating.

Remark: Unless otherwise specified, the characteristics of alternated pins are the same as those of port pins.

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Power supply input voltage	V_{DD} EV_{DD}			1.8		5.5	V
Power ground input voltage	V_{SS} EV_{SS}			-0.3			V
Input voltage, high	V_{IH1}	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41, P50~P51, P62~P63, P70~P75, P120~P124, EXCLK, EXCLKS, RESETB, P130, P136, P137, P140, P146, P147	Schmitt input	0.8V_{DD}		V_{DD}	V
	V_{IH2}	P60~P61		0.7V_{DD}		6.0	V
Input voltage, low	V_{IL1}	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41, P50~P51, P62~P63, P70~P75, P120~P124, EXCLK, EXCLKS, RESETB, P130, P136, P137, P140, P146, P147	Schmitt input	0		0.2V_{DD}	V
	V_{IL2}	P60~P61		0		0.3V_{DD}	V

Remark: Unless otherwise specified, the characteristics of alternated pins are the same as those of port pins.

(T_A=–40 ~ +105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Output voltage, high	V_{OH1}	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41, P50~P51, P62~P63, P70~P75, P120, P130, P136, P137, P140, P146, P147	4.0V≤V_{DD}≤5.5V, I_{OH1}=–12.0mA	V_{DD}–1.5			V
			4.0V≤V_{DD}≤5.5V, I_{OH1}=–6.0mA	V_{DD}–0.7			V
			2.4V≤V_{DD}≤5.5V, I_{OH1}=–3.0mA	V_{DD}–0.6			V
			1.8V≤V_{DD}≤5.5V, I_{OH1}=–2mA	V_{DD}–0.5			V
	V_{OH2}	P121~P124	4.0V≤V_{DD}≤5.5V, I_{OH2}=–2.5mA	V_{DD}–1.5			V
			4.0V≤V_{DD}≤5.5V, I_{OH2}=–1.5mA	V_{DD}–0.7			V
			2.4V≤V_{DD}≤5.5V, I_{OH2}=–0.5mA	V_{DD}–0.6			V
			1.8V≤V_{DD}≤5.5V, I_{OH2}=–0.4mA	V_{DD}–0.5			V
Output voltage, low	V_{OL1}	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41, P50~P51, P60~P63, P70~P75, P120, P130, P136, P137, P140, P146, P147	4.0V≤V_{DD}≤5.5V, I_{OL1}=35.0mA			1.2	V
			4.0V≤V_{DD}≤5.5V, I_{OL1}=20.0mA			0.7	V
			2.4V≤V_{DD}≤5.5V, I_{OL1}=9.0mA			0.4	V
			1.8V≤V_{DD}≤5.5V, I_{OL1}=6.0mA			0.4	V
	V_{OL2}	P121~P124	4.0V≤V_{DD}≤5.5V, I_{OL2}=10.0mA			1.2	V
			4.0V≤V_{DD}≤5.5V, I_{OL2}=6.0mA			0.7	V
			2.4V≤V_{DD}≤5.5V, I_{OL2}=2.5mA			0.4	V
			1.8V≤V_{DD}≤5.5V, I_{OL2}=1.5mA			0.4	V

Remark: Unless otherwise specified, the characteristics of alternated pins are the same as those of port pins.

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input leakage current, high	I_{LIH1}	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41, P50~P51, P60~P63, P70~P75, P120, P130, P136, P137, P140, P146, P147	V_I=V_{DD}			1	μA
	I_{LIH2}	RESETB	V_I=V_{DD}			1	μA
	I_{LIH3}	P121~P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I=V_{DD}, when an input port and an external clock are inputting			1	μA
			V_I=V_{DD}, when connecting a resonator			10	μA
Input leakage current, low	I_{LIL1}	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41, P50~P51, P60~P63, P70~P75, P120, P130, P136, P137, P140, P146, P147	V_I=V_{SS}			-1	μA
	I_{LIL2}	RESETB	V_I=V_{SS}			-1	μA
	I_{LIL3}	P121~P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	V_I=V_{SS}, when an input port and an external clock are inputting			-1	μA
			V_I=V_{SS}, when connecting a resonator			-10	μA
Internal pull-up resistance	R_U	P00~P01, P10~P17, P20~P27, P30~P31, P40~P41,	V_I=V_{SS}, when inputting a port	10	30	100	KΩ

		P50~P51, P62~P63, P70~P75, P120, P130, P136, P137, P140, P146, P147					
Internal pull-down resistance	R_D	P00~P01, P10~P17, P20~P27, P30~P31, P50~P51, P62~P63, P70~P75, P120, P130, P136, P137, P140, P146, P147	$V_I=V_{DD}$, when inputting a port	10	30	100	KΩ

Remark: Unless otherwise specified, the characteristics of alternated pins are the same as those of port pins.

6.5.2 Supply Current Characteristics

(T_A=−40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Run mode	High-speed on-chip oscillator	f_{HOCO}=64MHz,f_{IH}=64MHz Note 3			4.2	8.4	mA
				f_{HOCO}=48MHz,f_{IH}=48MHz Note 3			4.0	5.8	
			High-speed main system clock	f_{MX}=20MHz Note 2	Square wave input		1.8	3.6	mA
					Crystal oscillator connection		1.8	3.6	
			Subsystem clock operation	f_{SUB}=32.768KHz Note 4	Square wave input		70	85	uA
					Crystal oscillator connection		70	85	
			Low-speed on-chip oscillator	f_{IL}=15KHz Note 8			70	85	uA
	I_{DD2}	Sleep mode	High-speed on-chip oscillator	f_{HOCO}=64MHz, f_{IH}=64MHz Note 3			1.8	4.6	mA
				f_{HOCO}=48MHz, f_{IH}=48MHz Note 3			1.5	3.1	
			High-speed main system clock	f_{MX}=20MHz Note 2	Square wave input		0.9	1.8	mA
					Crystal oscillator connection		0.9	1.8	
			Subsystem clock operation	f_{SUB}=32.768KHz Note 5	Square wave input		1.1	16.5	uA
					Crystal oscillator connection		1.1	16.5	
			Low-speed on-chip oscillator	f_{IL}=15KHz Note 8			1.2	17	uA
	I_{DD3} Note 6	Deep sleep mode Note7	T_A=−40℃~+25℃ V_{DD}=3.0V				1.0	1.8	uA
			T_A=−40℃~+85℃ V_{DD}=3.0V				1.0	8.0	
			T_A=−40℃~+105℃ V_{DD}=3.0V				1.0	20	

Note 1: This is the current flowing through V_{DD}, including the input leakage current when the input pins are fixed to either V_{DD} or V_{SS}. Typical value: The CPU is in a NOP instruction loop and does not include peripheral operating current. Maximum value: The CPU is in a NOP instruction loop and includes peripheral operating current, but does not include current flowing to the A/D converter, LVD circuit, I/O ports, internal pull-up or pull-down resistors, or current during flash memory data rewriting.

Note 2: This is the case where the high-speed on-chip oscillator and the subsystem clock stop oscillating.

Note 3: This is the case where the high-speed main system clock and the subsystem clock stop oscillating.

Note 4: This is the case where the high-speed on-chip oscillator and the high-speed main system clock stop oscillating.

Note 5: This is the case where the high-speed on-chip oscillator and the high-speed main system clock stop oscillating. It includes the current flowing to the RTC, but does not include the current flowing to the 15-bit interval timer and watchdog timer.

Note 6: Does not include the current flowing to the RTC, 15-bit interval timer, and watchdog timer.

Note 7: For the current value when the subsystem clock operates in deep sleep mode, please refer to the current value when the subsystem clock operates in sleep mode.

Note 8: This is the case where the high-speed on-chip oscillator, high-speed main system clock, and subsystem clock stop oscillating.

Remarks:

1. f_{HOCO}: High-speed on-chip oscillator clock frequency
   f_{IH}: High-speed on-chip oscillator system clock frequency
2. f_{SUB}: External subsystem clock frequency (XT1/XT2 oscillator frequency)
3. f_{MX}: External main system clock frequency (X1/X2 oscillator frequency)
4. f_{IL}: Low-speed on-chip oscillator clock frequency
5. The typical value temperature condition is T_A = 25°C.

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Low speed on-chip oscillator operating current	I_{FIL} Note 1				0.2		uA
RTC operating current	I_{RTC} Note 1,2,3				0.04		uA
15-bit interval timer operating current	I_{IT} Note 1,2,4				0.02		uA
Watchdog timer operating current	I_{WDT} Note 1,2,5	f_{IL}=15KHz			0.22		uA
A/D converter operating current	I_{ADC} Note 1,6	ADC HS mode @64MHz			2.2		mA
		ADC HS mode @4MHz			1.3		mA
		ADC LC mode @24MHz			1.1		mA
		ADC LC mode @4MHz			0.8		mA
PGA operating current		Per channel			480	750	uA
Comparator operating current	I_{CMP} Note 1,9	Per channel	No internal reference voltage is used		60	100	uA
			An internal reference voltage is used		80	140	uA
LVD operating current	I_{LVD} Note 1,7				0.08		uA

Note 1: This is the current flowing through V_{DD}.

Note 2: This refers to the situation where the high-speed on-chip oscillator and the high-speed system clock stop oscillating.

Note 3: This refers to the current flowing only to the Real-Time Clock (RTC) (excluding the current consumed by the low-speed on-chip oscillator and the XT1 oscillator circuit). When the RTC is running in either the run mode or sleep mode, the microcontroller's current value is the sum of I_{DD1} or I_{DD2} and I_{RTC}. Additionally, when the low-speed on-chip oscillator is selected, I_{FIL} must be added. The I_{DD2} value during the operation of the sub-system clock includes the current consumed by the RTC.

Note 4: This refers to the current flowing only to the 15-bit interval timer (excluding the current consumed by the low-speed on-chip oscillator and the XT1 oscillator circuit). When the 15-bit interval timer is running in either the run mode or sleep mode, the microcontroller's current value is the sum of I_{DD1} or I_{DD2} and I_{IT}. Additionally, when the low-speed on-chip oscillator is selected, I_{FIL} must be added.

Note 5: This refers to the current flowing only to the watchdog timer (including the current consumed by the low-speed on-chip oscillator). When the watchdog timer is running, the microcontroller's current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{WDT}.

Note 6: This refers to the current flowing only to the A/D converter. When the A/D converter is running in either the run mode or sleep mode, the microcontroller's current value is the sum of I_{DD1} or I_{DD2} and I_{ADC}.

Note 7: This refers to the current flowing only to the Low Voltage Detection (LVD) circuit. When the LVD circuit is running, the microcontroller's current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{LVD}.

Note 8: This refers to the current flowing only to the D/A converter. When the D/A converter is running in either the run mode or sleep mode, the microcontroller's current value is the sum of I_{DD1} or I_{DD2} and I_{DAC}.

Note 9: This refers to the current flowing only to the comparator circuit. When the comparator circuit is running, the microcontroller's current value is the sum of I_{DD1}, I_{DD2}, or I_{DD3} and I_{CMP}.

Remarks:

1. f_{IL}: Low-speed on-chip oscillator clock frequency
2. The typical value temperature condition is T_A = 25°C.

6.6 AC Characteristics

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (F_{MAIN}) operation	1.8V≤V_{DD}≤5.5V	0.015625		1	us
		Subsystem clock (F_{SUB}) operation	1.8V≤V_{DD}≤5.5V	28.5	30.5	31.3	us
External system clock frequency	F_{EX}	1.8V≤V_{DD}≤5.5V		1.0		20.0	MHz
	F_{EXS}	1.8V≤V_{DD}≤5.5V		32.0		35.0	KHz
High/low width of external system clock input	T_{EXH}, T_{EXL}	1.8V≤V_{DD}≤5.5V		24			ns
	T_{EXHS}, T_{EXLS}	1.8V≤V_{DD}≤5.5V		13.7			us
TI00 ~TI03, TI10 ~TI13 inputs high-level width, low-level width	T_{TIH}, T_{TIL}	1.8V≤V_{DD}≤5.5V		1/F_{MCK}+10			ns
TO00 ~ TO03, TO10 ~ TO13 output frequency	F_{TO}	4.0V≤V_{DD}≤5.5V				16	MHz
		2.4V≤V_{DD}＜4.0V				8	MHz
		1.8V≤V_{DD}＜2.4V				4	MHz
CLKBUZ0, CLKBUZ1 output frequency	F_{PCL}	4.0V≤V_{DD}≤5.5V				16	MHz
		2.4V≤V_{DD}＜4.0V				8	MHz
		1.8V≤V_{DD}＜2.4V				4	MHz
Interrupt input high-level width, low-level width	T_{INTH}, T_{INTL}	INTP0 ~ INTP3	1.8V≤V_{DD}≤5.5V	1			us
Key interrupt input high-level width, low-level width	T_{KR}	KR0 ~ KR5	1.8V≤V_{DD}≤5.5V	250			ns
RESETB low-level width	T_{RSL}			10			us

Remark: F_{MCK}: Timer4 operating clock frequency

6.7 Peripheral Function Characteristics

6.7.1 Universal Interface Unit

1) UART mode

(T_A=–40~+85℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Condition		Specification value		Unit
			Min.	Max.	
Transfer rate	1.8V ≤ V_{DD} ≤ 5.5V			F_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{MCK}=f_{CLK}		10.6	Mbps

(T_A=+85~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Condition		Specification value		Unit
			Min.	Max.	
Transfer rate	1.8V ≤ V_{DD} ≤ 5.5V			F_{MCK}/12	bps
		Theoretical value of the maximum transfer rate f_{MCK}=f_{CLK}		5.3	Mbps

2) 3-wire SPI mode (master mode, internal clock output)

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		–40 ~ +85℃		+85 ~ +105℃		Unit
				Min.	Max.	Min.	Max.	
SCLKp cycle time	T_{KCY1}	T_{KCY1} ≥2/F_{CLK}	4.0V ≤V_{DD} ≤ 5.5V	31.25		62.5		ns
			2.7V ≤V_{DD} ≤ 5.5V	41.67		83.33		
			2.4V ≤ V_{DD} ≤ 5.5V	65		125		ns
			1.8V ≤ V_{DD} ≤ 5.5V	125		250		ns
SCLKp high/low level width	T_{KH1}, T_{KL1}	4.0V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2–4		T_{KCY1}/2–7		ns
		2.7V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2–5		T_{KCY1}/2–10		ns
		2.4V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2–10		T_{KCY1}/2–20		ns
		1.8V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2–19		T_{KCY1}/2–38		ns
SDIp set-up time (for SCLKp↑)	T_{SIK1}	4.0V ≤ V_{DD} ≤ 5.5V		12		23		ns
		2.7V ≤ V_{DD} ≤ 5.5V		17		33		ns
		2.4V ≤ V_{DD} ≤ 5.5V		20		38		ns
		1.8V ≤ V_{DD} ≤ 5.5V		28		55		ns
SDIp hold time (for SCLKp↑)	T_{KSI1}	1.8V ≤ V_{DD} ≤ 5.5V		5		10		ns
Delay time from SCLKp↓→ SDOp	T_{KSO1}	1.8V ≤ V_{DD} ≤ 5.5V C=20pF Note 1			5		10	ns

Note 1: C is the load capacitance of the SCLKp and SDOp output lines.

Caution: By using the port input mode register and the port output mode register, select the SDIp pin as the normal input buffer and select the SDOp and SCLKp pins as the normal output mode.

3) 3-wire SPI mode (slave mode, external clock input)

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		–40 ~ +85℃		+85 ~ +105℃		Unit
				Min.	Max.	Min.	Max.	
SCLKp cycle time	T_{KCY2}	4.0V ≤ V_{DD} ≤ 5.5V	20MHz < F_{MCK}	8/ F_{MCK}		16/ F_{MCK}		ns
			F_{MCK} ≤20MHz	6/ F_{MCK}		12/ F_{MCK}		ns
		2.7V ≤ V_{DD} ≤ 5.5V	16MHz < F_{MCK}	8/ F_{MCK}		16/ F_{MCK}		ns
			F_{MCK} ≤16MHz	6/ F_{MCK}		12/ F_{MCK}		ns
		2.4V ≤ V_{DD} ≤ 5.5V		6/F_{MCK} and ≥500	-	12/F_{MCK} and ≥1000		ns
		1.8V ≤ V_{DD} ≤ 5.5V		6/F_{MCK} and ≥750	-	12/F_{MCK} and ≥1500		ns
SCLKp high/low level width	T_{KH2}, T_{KL2}	4.0V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-7		T_{KCY1}/2-14		ns
		2.7V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-8		T_{KCY1}/2-16		ns
		1.8V ≤ V_{DD} ≤ 5.5V		T_{KCY1}/2-18		T_{KCY1}/2-36		ns
SDIp set-up time (for SCLKp↑)	T_{SIK2}	2.7V ≤ V_{DD} ≤ 5.5V		1/F_{MCK}+20		1/F_{MCK} +40		ns
		1.8V ≤ V_{DD} ≤ 5.5V		1/F_{MCK}+30		1/F_{MCK} +60		ns
SDIp hold time (for SCLKp↑)	T_{KSI2}	1.8V ≤ V_{DD} ≤ 5.5V		1/F_{MCK}+31		1/F_{MCK} +62		ns
Delay time from SCLKp↓→SDOp	T_{KSO2}	2.7V ≤ V_{DD} ≤ 5.5V C=30pF Note 1			2/F_{MCK}+ 44		2/F_{MCK}+ 66	ns
		2.4V ≤ V_{DD} ≤ 5.5V C=30pF Note 1			2/F_{MCK}+ 75		2/F_{MCK}+ 113	ns
		1.8V ≤ V_{DD} ≤ 5.5V C=30pF Note 1			2/F_{MCK}+ 100		2/F_{MCK}+ 150	ns

Note 1: C is the load capacitance of the SCLKp and SDOp output lines.

Caution: By using the port input mode register and the port output mode register, select the SDIp pin and the SCLKp pin as normal input buffers, and select the SDOp pin as the normal output mode.

4) 4-wire SPI mode (slave mode, external clock input)

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition		–40 ~ +85℃		+85 ~ +105℃		Unit
				Min.	Max.	Min.	Max.	
SSI00 set-up time	tSSIK	DAPmn=0	2.7V ≤ V_{DD} ≤ 5.5V	120		240		ns
			1.8V ≤ V_{DD} ≤ 5.5V	200		400		ns
		DAPmn=1	2.7V ≤ V_{DD} ≤ 5.5V	1/F_{MCK}+120	-	1/F_{MCK}+240		ns
			1.8V ≤ V_{DD} ≤ 5.5V	1/F_{MCK}+200	-	1/F_{MCK}+400		ns
SSI00 hold time	tKSSI	DAPmn=0	2.7V ≤ V_{DD} ≤ 5.5V	1/F_{MCK}+120	-	1/F_{MCK}+240		ns
			1.8V ≤ V_{DD} ≤ 5.5V	1/F_{MCK}+200	-	1/F_{MCK}+400		ns
		DAPmn=1	2.7V ≤ V_{DD} ≤ 5.5V	120		240		ns
			1.8V ≤ V_{DD} ≤ 5.5V	200		400		ns

Caution: By using the port input mode register and the port output mode register, select the SDIp pin and the SCLKp pin as normal input buffers, and select the SDOp pin as the normal output mode

5) Simplified IIC mode

(T_A=–40~+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

Item	Symbol	Condition	–40 ~ +85℃		+85 ~ +105℃		Unit
			Min.	Max.	Min.	Max.	
SCLr clock frequency	f_{SCL}	2.7V ≤ V_{DD} ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ		1000[Note 1]		400[Note 1]	KHz
		1.8V ≤ V_{DD} ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ		400[Note 1]		100[Note 1]	KHz
		1.8V ≤ V_{DD} ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ		300[Note 1]		75[Note 1]	KHz
Hold time when SCLr is low	t_{LOW}	2.7V ≤ V_{DD} ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	475		1200		ns
		1.8V ≤ V_{DD} ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1150		4600		ns
		1.8V ≤ V_{DD} ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1550		6500		ns
Hold time when SCLr is high	t_{HIGH}	2.7V ≤ V_{DD} ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	475		1200		ns
		1.8V ≤ V_{DD} ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1150		4600		ns
		1.8V ≤ V_{DD} ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1550		6500		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7V ≤ V_{DD} ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	1/F_{MCK}+85[Note 2]	-	1/F_{MCK}+220[Note 2]		ns
		1.8V ≤ V_{DD} ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1/F_{MCK}+145[Note 2]	-	1/F_{MCK}+580[Note 2]		ns
		1.8V ≤ V_{DD} ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1/F_{MCK}+230[Note 2]	-	1/F_{MCK}+1200[Note 2]		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7V ≤ V_{DD} ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ		305		770	ns
		1.8V ≤ V_{DD} ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ		355		1420	ns
		1.8V ≤ V_{DD} ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ		405		2070	ns

Note 1: It must be set to at least F_{MCK}/4.

Note 2: The setting value of F_{MCK} cannot exceed the hold time for SCLr = “L” and SCLr = “H”.

6.7.2 Serial Interface IICA

1) I²C standard mode

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLA0 clock frequency	F_{SCL}	Standard mode: F_{CLK}≥1MHz		100	KHz
Set-up time of the start condition	$T_{SU: STA}$		4.7		us
Hold time of the start condition Note1	$T_{HD: STA}$		4.0		us
Hold time when SCLA0 is low	T_{LOW}		4.7		us
Hold time when SCLA0 is high	T_{HIGH}		4.0		us
Data set-up time (reception)	$T_{SU: DAT}$		250		ns
Data hold time (transmission) Note2	$T_{HD: DAT}$		0	3.45	us
Set-up time of the stop condition	$T_{SU: STO}$		4.0		us
Bus idle time	T_{BUF}		4.7		us

Note 1: Generate the first clock pulse after generating the start condition or re-start condition.

Note 2: The maximum value of $t_{HD: DAT}$ must be ensured during normal data transfer, and a wait is required during acknowledgment (ACK).

Remark: The maximum value of Cb (communication line capacitance) for each mode and the corresponding Rb (pull-up resistor value of the communication line) are as follows:

Standard mode: Cb=400pF, Rb=2.7kΩ

2) I²C fast mode

(TA=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLA0 clock frequency	F_{SCL}	Fast mode: F_{CLK}≥3.5MHz		400	KHz
Set-up time of the start condition	$T_{SU: STA}$		0.6		us
Hold time of the start condition Note1	$T_{HD: STA}$		0.6		us
Hold time when SCLA0 is low	T_{LOW}		1.3		us
Hold time when SCLA0 is high	T_{HIGH}		0.6		us
Data set-up time (reception)	$T_{SU: DAT}$		100		ns
Data hold time (transmission) Note2	$T_{HD: DAT}$		0	0.9	us

Set-up time of the stop condition	$T_{SU: STO}$		0.6		us
Bus idle time	T_{BUF}		1.3		us

Note 1: Generate the first clock pulse after generating the start condition or re-start condition.

Note 2: The maximum value of $T_{HD: DAT}$ must be ensured during normal data transfer, and a wait is required during acknowledgment (ACK).

Remark: The maximum value of Cb (communication line capacitance) for each mode and the corresponding Rb (pull-up resistor value of the communication line) are as follows:

Fast mode: Cb=320pF, Rb=1.1kΩ

3) I^2C enhanced fast mode

(TA=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Specification value		Unit
			Min.	Max.	
SCLA0 clock frequency	F_{SCL}	Enhanced fast mode: F_{CLK}≥10MHz		1000	KHz
Set-up time of the start condition	$T_{SU: STA}$		0.26		us
Hold time of the start condition Note1	$T_{HD: STA}$		0.26		us
Hold time when SCLA0 is low	T_{LOW}		0.5		us
Hold time when SCLA0 is high	T_{HIGH}		0.26		us
Data set-up time (reception)	$T_{SU: DAT}$		50		ns
Data hold time (transmission) Note2	$T_{HD: DAT}$		0	0.45	us
Set-up time of the stop condition	$T_{SU: STO}$		0.26		us
Bus idle time	T_{BUF}		0.5		us

Note 1: Generate the first clock pulse after generating the start condition or re-start condition.

Note 2: The maximum value of $T_{HD: DAT}$ must be ensured during normal data transfer, and a wait is required during acknowledgment (ACK).

Remark: The maximum value of Cb (communication line capacitance) for each mode and the corresponding Rb (pull-up resistor value of the communication line) are as follows:

Enhanced fast mode: Cb=120pF, Rb=1.1kΩ

6.8 Analog Characteristics

6.8.1 A/D Converter Characteristics

Classification of A/D converter characteristics

Input channel \ Reference voltage	Reference voltage (+)=AV_{REFP} Reference voltage (-)=AV_{REFM}	Reference voltage (+)=V_{DD} Reference voltage (-)=V_{SS}
ANI0~ANI36	See 6.8.1(1).	See 6.8.1 (2).
Internal reference voltage, temperature sensor output voltage		

(1) When selecting reference voltage (+)=AV_{REFP}/ANI0, reference voltage (-)=AV_{REFM}/ANI1
(T_A= -40~105℃, 1.8V≤AV_{REFP}≤V_{DD}≤5.5V, V_{SS}=0V, reference voltage (+)=AV_{REFP}, reference voltage (-)= AV_{REFM} =0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES	-		-	12	-	bit
Overall error Note 1	ET	12-bit resolution	1.8V ≤ AV_{REFP}≤ 5.5V	-	3	-	LSB
Zero-scale error Note 1	E_{ZS}	12-bit resolution	1.8V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Full-scale error Note 1	E_{FS}	12-bit resolution	1.8V ≤AV_{REFP}≤ 5.5V	-	0	-	LSB
Integral linearity error Note 1	EL	12-bit resolution	1.8V ≤AV_{REFP}≤ 5.5V	-1	-	1	LSB
Differential linearity error Note 1	ED	12-bit resolution	1.8V ≤AV_{REFP}≤ 5.5V	-1.5	-	1.5	LSB
Conversion time Note 3	T_{CONV}	12-bit resolution Conversion target: ANI2~ ANI36	1.8V ≤V_{DD}≤ 5.5V	45	-	-	1/F_{ADC}
		12-bit resolution Conversion target: Internal reference voltage, temperature sensor output voltage, PGA output voltage	1.8V ≤V_{DD}≤ 5.5V	72	-	-	1/F_{ADC}
External input resistance	R_{AIN}	R_{AIN}＜ (Ts / (F_{ADC} x C_{ADC} x ln (2^{12+2}))- R_{ADC})		-	7.5 Note 4	-	KΩ
Sample switching resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample-and-hold capacitance	C_{ADC}	-		-	2	-	pF
Analog input voltage	V_{AIN}	ANI2~ANI36		0	-	AV_{REF}	V
		Internal reference voltage (1.8V≤V_{DD}≤5.5V)		V_{BGR} Note 2			V
		Temperature sensor output voltage (1.8V≤V_{DD}≤5.5V)		V_{TMPS25} Note 2			V

Note 1: Quantization error (±1/2 LSB) is not included.

Note 2: Please refer to “6.8.2 Characteristics of Temperature Sensor/Internal Reference Voltage”.

Note 3: F_{ADC} refers to the action frequency of the AD, with the maximum action frequency being 48 MHz.

Note 4: This specification is guaranteed by the design, and is not tested in mass production. The typical default sampling period is Ts = 13.5, and the conversion speed is fad = 64MHz under the given conditions.

(2) When selecting reference voltage (+)=V_{DD}, reference voltage (–)=V_{SS}

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}= 0V, reference voltage (+)=V_{DD}, reference voltage (-)=V_{SS})

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Resolution	RES	-		-	12	-	bit
Overall error Note 1	ET	12-bit resolution	1.8V ≤AV_{REFP}≤5.5V	-	6	-	LSB
Zero-scale error Note 1	E_{ZS}	12-bit resolution	1.8V ≤AV_{REFP}≤5.5V	-	0	-	LSB
Full-scale error Note 1	E_{FS}	12-bit resolution	1.8V ≤AV_{REFP}≤5.5V	-	0	-	LSB
Integral linearity error Note 1	EL	12-bit resolution	1.8V ≤AV_{REFP}≤5.5V	-2	-	2	LSB
Differential linearity error Note 1	ED	12-bit resolution	1.8V ≤AV_{REFP}≤5.5V	-3	-	3	LSB
Conversion time Note 3	T_{CONV}	12-bit resolution Conversion target: ANI0~ANI36	1.8V≤V_{DD}≤5.5V	45	-	-	1/F_{ADC}
		12-bit resolution Conversion target: Internal reference voltage, temperature sensor output voltage, PGA output voltage	1.8V≤V_{DD}≤5.5V	72	-	-	1/F_{ADC}
External input resistance	R_{AIN}	R_{AIN} ＜ (T_S / (F_{ADC} x C_{ADC} x ln (2^{12+2}))- R_{ADC})		-	7.5 Note4	-	KΩ
Sample switching resistance	R_{ADC}	-		-	-	1.5	KΩ
Sample-and-hold capacitance	C_{ADC}	-		-	2	-	pF
Analog input voltage	V_{AIN}	ANI0~ANI36		0	-	V_{DD}	V
		Internal reference voltage (1.8V≤V_{DD}≤5.5V)		V_{BGR} Note 2			V
		Temperature sensor output voltage (1.8V≤V_{DD}≤5.5V)		V_{TMPS} Note 2			V

Note 1: Quantization error (±1/2 LSB) is not included.

Note 2: Please refer to “6.8.2 Characteristics of Temperature Sensor/Internal Reference Voltage”.

Note 3: F_{ADC} refers to the action frequency of the AD, with the maximum action frequency being 48 MHz.

Note 4: This specification is guaranteed by the design, and is not tested in mass production. The typical default sampling period is Ts = 13.5, and the conversion speed is F_{ADC}= 64MHz under the given conditions.

6.8.2 Characteristics of Temperature Sensor/Internal Reference Voltage

(T_A= -40~105℃, 1.8V≤V_{DD}≤5.5V, V_{SS} =0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	V_{TMPS25}	T_A=25℃	-	1.09	-	V
Internal reference voltage	V_{BGR}	T_A= -40~10℃	1.25	1.45	1.65	V
		T_A=10~70℃	1.38	1.45	1.52	V
		T_A=70~105℃	1.35	1.45	1.55	V
Temperature coefficient	F_{VTMPS}	-	-	-3.5	-	mV/℃
Operation stabilization wait time	T_{AMP}	-	5	-	-	us

Note: Low temperature specification is guaranteed by the design, and is not tested in mass production.

6.8.3 Comparator

(T_A= -40~ 105℃, 1.8V≤V_{DD}≤5.5V, V_{SS} =0V)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Input offset voltage	V_{OFFSET}	-		-	±10	±40	mV
Input voltage range	V_{IN}	-		0	-	V_{DD}	V
Internal reference voltage offset	ΔV_{IREF}	CmRVM register: 7FH~80H (m=0,1)		-	-	±2	LSB
		Others		-		±1	LSB
Response time	T_{CR}, T_{CF}	Input amplitude±100mV		-	70	150	ns
Operation stabilization time Note1	T_{STB}	CMPn=0->1	V_{DD}=3.3~5.5V	-	-	1	us
			V_{DD}=1.8~3.3V	-	-	3	
Reference voltage stabilization time	T_{VR}	CVRE=0->1 Note 2		-	-	20	us
Operating current	I_{CMPDD}	See “6.5.2 Supply Current Characteristics”.					

Note 1: The time required from enabling the comparator (CMPnEN = 0 → 1) to meet the DC/AC specification requirements of the comparator.

Note 2: After enabling the internal reference voltage generator (by setting the CVREm bit to 1; m = 0 to 1), the comparator output (CnOE bit = 1; n = 0 to 1) can only be enabled after the reference voltage stabilizes.

6.8.4 Programmable Gain Amplifier (PGA)

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input offset voltage	V_{IOPGA}				±3	±10	mV
Input voltage range	V_{IPGA}			0		0.9xV_{DD}/ Gain	V
Output voltage range	V_{IOHPGA}			0.93xV_{DD}			V
	V_{IOLPGA}					0.07xV_{DD}	V
Gain error	EG	x4				±1	%
		x8				±1	%
		x10				±1	%
		x12				±2	%
		x14				±2	%
		x16				±2	%
		x32				±3	%
Conversion rate	SR_{RPGA}	Rising Vin= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 10 to 90% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5			V/us
			4.0 V ≤ V_{DD} ≤ 5.5 V (x32)	3.0			
			2.0 V ≤ V_{DD} ≤ 4.0V	0.5			
	SR_{FPGA}	Falling Vin= 0.1V_{DD}/gain to 0.9V_{DD}/gain. 90 to 10% of output voltage amplitude	4.0 V ≤ V_{DD} ≤ 5.5 V (Other than x32)	3.5			
			4.0 V ≤ V_{DD} ≤ 5.5 V (x32)	3.0			
			2.0 V ≤ V_{DD} ≤ 4.0V	0.5			
Stable operation time[Note 1]	T_{PGA}	x4				5	us
		x8				5	us
		x10				5	us
		x12				10	us
		x14				10	us
		x16				10	us
		x32				10	us
Operating current	I_{PGADD}	See “6.5.2 Supply Current Characteristics”.					

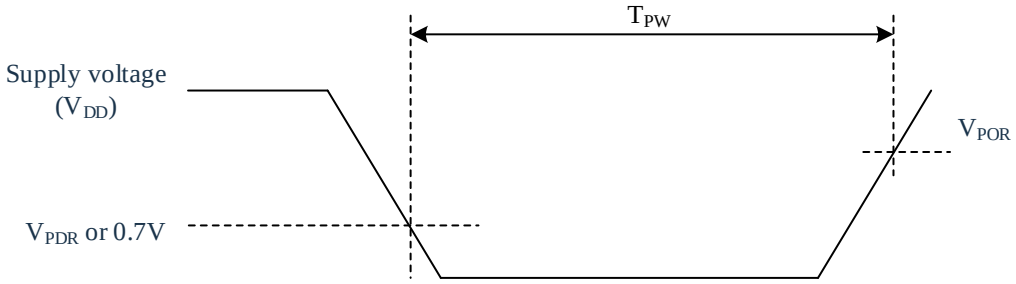
Note 1: The time required from enabling the PGA (PGAEN = 1) to meeting the DC and AC specification requirements of the PGA.

6.8.5 POR Characteristics

(T_A= -40~+105°C, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detect voltage	V_{POR}	When the supply voltage rises		1.65	1.75	V
	V_{PDR}	When the supply voltage drops	1.37	1.49		V
Minimum pulse width Note1	T_{PW}	-	300			us

Note 1: This is the time required for the POR reset when V_{DD} drops below V_{PDR}. Additionally, in deep sleep mode, when the main system clock (F_{MAIN}) oscillation is stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) of the clock operation status control register (CSC), it is the time required for the POR reset from when V_{DD} drops below 0.7V to when it rises above V_{POR}.



6.8.6 LVD Characteristics

1) Reset mode and interrupt mode

(T_A= -40~105℃, V_{PDR}≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection voltage	V_{LVD0}	The power supply voltage is rising.		3.97	4.08	V
		The power supply voltage is falling.	3.81	3.9		V
	V_{LVD1}	The power supply voltage is rising.		3.68		V
		The power supply voltage is falling.		3.61		V
	V_{LVD2}	The power supply voltage is rising.		3.12		V
		The power supply voltage is falling.		3.06		V
	V_{LVD3}	The power supply voltage is rising.		3.01		V
		The power supply voltage is falling.		2.96		V
	V_{LVD4}	The power supply voltage is rising.		2.92		V
		The power supply voltage is falling.		2.86		V
	V_{LVD5}	The power supply voltage is rising.		2.81		V
		The power supply voltage is falling.		2.75		V
	V_{LVD6}	The power supply voltage is rising.		2.71		V
		The power supply voltage is falling.		2.65		V
	V_{LVD7}	The power supply voltage is rising.		2.61		V
		The power supply voltage is falling.		2.55		V
	V_{LVD8}	The power supply voltage is rising.		2.5		V
		The power supply voltage is falling.		2.45		V
	V_{LVD9}	The power supply voltage is rising.		2.09		V
		The power supply voltage is falling.		2.05		V
	V_{LVD10}	The power supply voltage is rising.		1.99		V
		The power supply voltage is falling.		1.95		V
	V_{LVD11}	The power supply voltage is rising.		1.89	1.91	V
		The power supply voltage is falling.	1.80	1.85		V
Minimum pulse width	t_{LW}		300			us
Detection delay					300	us

2) Interrupt & reset mode

(T_A= -40~155℃, V_{PDR} ≤V_{DD}≤5.5V, V_{SS}=0V)

Item	Symbol	Condition			Min.	Typ.	Max.	Unit
Interrupt & reset mode	V_{LVDA0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=0	Falling reset voltage		1.60	1.63		V
	V_{LVDA1}		LVIS1=1 LVIS0=0	Rising release reset voltage		1.77	1.81	V
				Falling interrupt voltage	1.70	1.73		V
	V_{LVDA2}		LVIS1=0 LVIS0=1	Rising release reset voltage		1.88		V
				Falling interrupt voltage		1.84		V
	V_{LVDA3}		LVIS1=0 LVIS0=0	Rising release reset voltage		2.92		V
				Falling interrupt voltage		2.86		V
	V_{LVDB0}	V_{POC2}=0 V_{POC1}=0 V_{POC0}=1	Falling reset voltage			1.84	-	V
	V_{LVDB1}		LVIS1=1 LVIS0=0	Rising release reset voltage		1.98		V
				Falling interrupt voltage		1.94		V
	V_{LVDB2}		LVIS1=0 LVIS0=1	Rising release reset voltage		2.09		V
				Falling interrupt voltage		2.04		V
	V_{LVDB3}		LVIS1=0 LVIS0=0	Rising release reset voltage		3.13		V
				Falling interrupt voltage		3.06		V
	V_{LVDC0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=0	Falling reset voltage			2.45		V
	V_{LVDC1}		LVIS1=1 LVIS0=0	Rising release reset voltage		2.61		V
				Falling interrupt voltage		2.55		V
	V_{LVDC2}		LVIS1=0 LVIS0=1	Rising release reset voltage		2.71		V
				Falling interrupt voltage		2.65		V
	V_{LVDC3}		LVIS1=0 LVIS0=0	Rising release reset voltage		3.75		V
				Falling interrupt voltage		3.67		V
	V_{LVDD0}	V_{POC2}=0 V_{POC1}=1 V_{POC0}=1	Falling reset voltage			2.75		V
	V_{LVDD1}		LVIS1=1 LVIS0=0	Rising release reset voltage		2.92		V
				Falling interrupt voltage		2.86		V
	V_{LVDD2}		LVIS1=0 LVIS0=1	Rising release reset voltage		3.02		V
				Falling interrupt voltage		2.96		V
	V_{LVDD3}		LVIS1=0 LVIS0=0	Rising release reset voltage		4.06	4.14	V
				Falling interrupt voltage	3.90	3.98		V

6.8.7 Reset Time and Power Supply Voltage Rise Slope Characteristics

(TA= -40~+105℃, V_{SS}=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Reset time	T_{RESET}			1		ms
Power supply voltage rise slope	SV_{DD}				54	V/ms

6.9 Memory Characteristics

6.9.1 Flash Memory

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Symbol	Parameter	Test condition	Min.	Max.	Unit
T_{PROG}	Word write time (32bit)	T_A = -40~105℃	24	30	us
T_{ERASE}	Sector erase time (512B)	T_A = -40~105℃	4	5	ms
	Chip erase time	T_A = -40~105℃	20	40	ms
N_{END}	Number of rewritable times	T_A = -40~105℃	100	-	Kcycles
T_{RET}	Data retention period	100 Kcyles[Note 1] at T_A = 105℃	20	-	Years

Note 1: The data is guaranteed by characterization results, and is not tested in production.

Note 2: Cycling performed over the whole temperature range.

6.9.2 RAM Memory

(T_A=–40~+105℃, 1.8V≤V_{DD}≤5.5V, V_{SS}=0V)

Symbol	Parameter	Test condition	Min.	Max.	Unit
$V_{RAMHOLD}$	RAM hold voltage	T_A = -40~105℃	0.8	-	V

6.10 EMS Characteristics

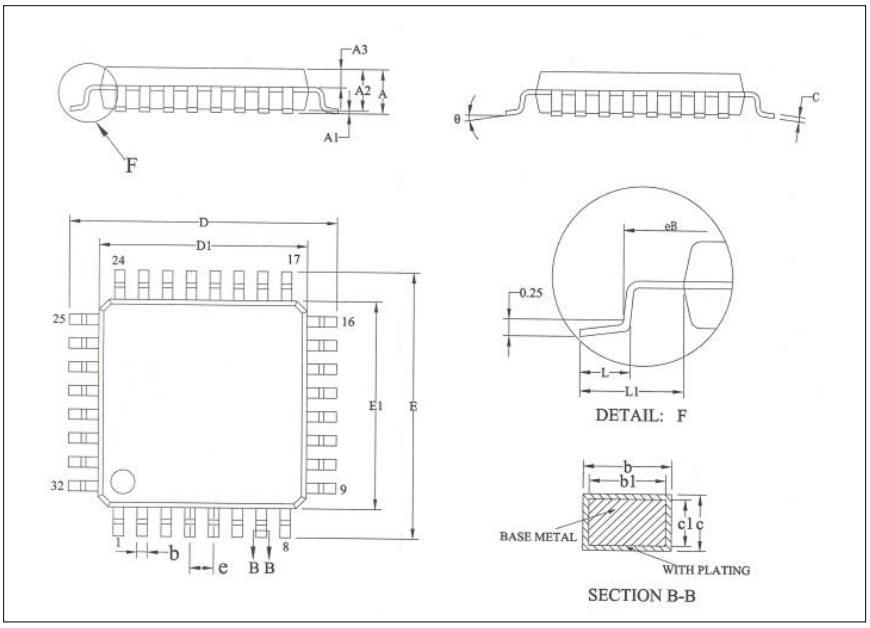
6.10.1 ESD Electrical Characteristics

Symbol	Parameter	Test condition	Grade
$V_{ESD(HBM)}$	Electrostatic discharge (Human-Body Model HBM)	TA = +25℃, JESD22-A114	3A

Note: The data is guaranteed by characterization results, and is not tested in production.

7 Package Dimensions

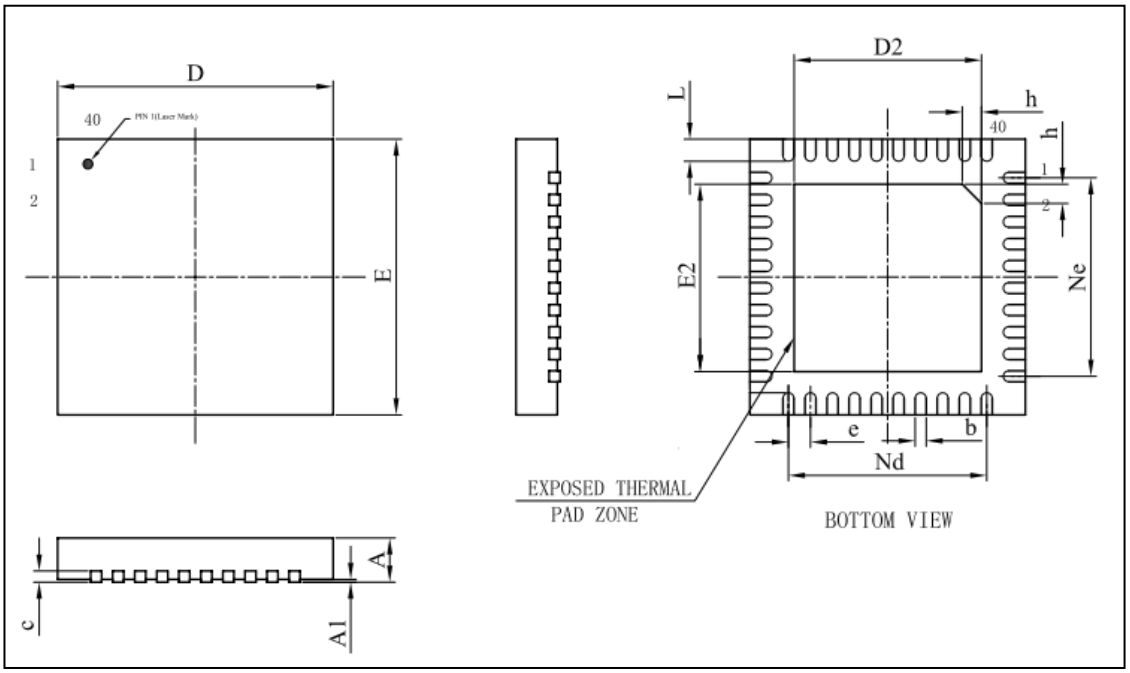
7.1LQFP32 (7x7mm, 0.8mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	-	0.43
b1	0.31	-	0.39
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

Caution: Package dimensions do not include mold flash or gate burrs.

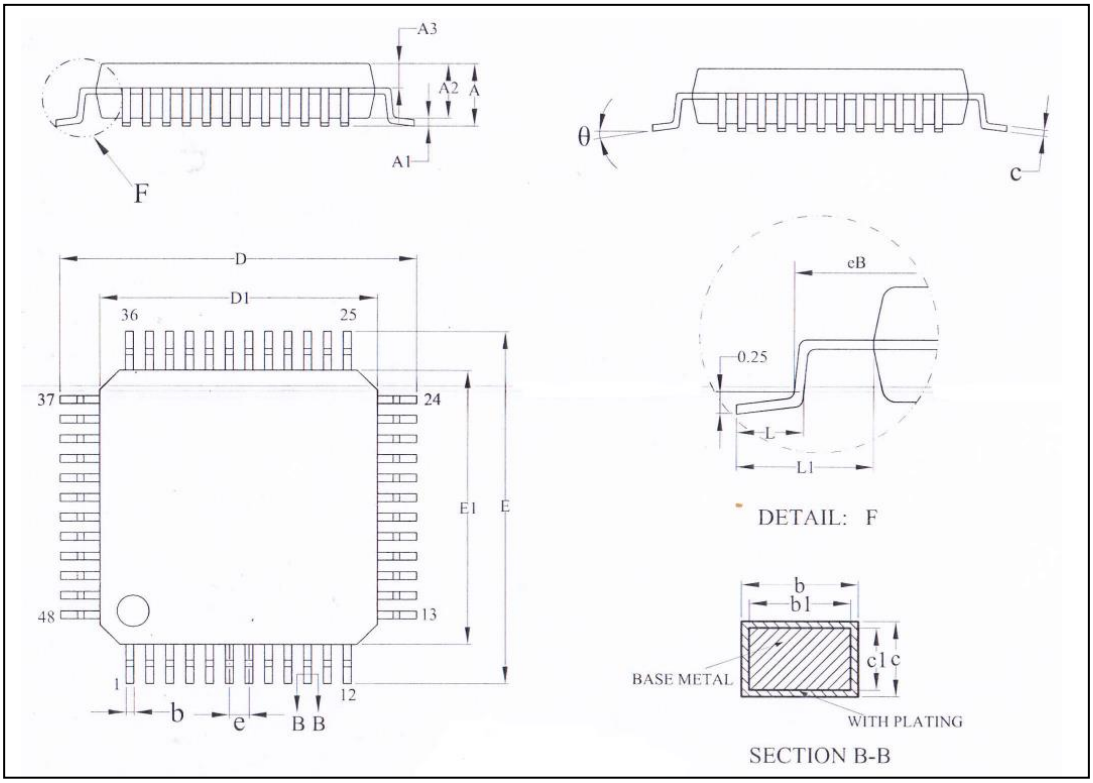
7.2 QFN40 (5x5x0.75mm-0.4mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.80
e	0.40BSC		
Ne	3.60BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	3.40	3.80
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Caution: Package dimensions do not include mold flash or gate burrs.

7.3LQFP48 (7x7mm, 0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.43	-	0.75
L1	1.00REF		
θ	0	-	8°

Caution: Package dimensions do not include mold flash or gate burrs.

8 Revision History

Version #	Date	Description of changes
V0.0.1	Nov. 2024	Initial release
V0.5.0	Nov. 2024	Changed “TBD” in Electrical Characteristics to measured results.
V0.5.1	Feb. 2025	1) Modified 1.3.3 Top View, and removed the default IICA function on pins P60 and P61. The pin mapping for this function needs to be configured via registers. 2) Modified the power consumption value in deep sleep mode in Section Features.
V0.5.2	2025.2.17	Removed the BAT32G135BGE32NA model and related information
V0.5.3	2025.5.29	Delete the wrong content in Chapter 5.21
	2025.06.04	Correction of IDD3 current magnitude and PGA operating current magnitude in the table in section 6.5.2
	2025.06.06	1) Delete the wrong content in Chapter 1.3.3 2) Update the package size information of QFN40