CMS32M55xx Datasheet

ARM® Cortex® -M0 32-bit motor microcontroller

Rev. 1.13

1. Product Features

1.1 MCU Functions

- **Built in ARM Cortex™-M0, 64MHz@2.1V~5.5V**
  - Single periodic 32-bit hardware multiplier
- **32-bit hardware divider (HWDIV)**
  - Signed/unsigned mode,6 HCLK to complete calculation
- **Memory**
  - Maximum 32K byte program FLASH(APROM + BOOT)
  - 1K byte FLASH data space (separated space)
  - Maximum 8K byte SRAM (support distributed write-protection)
  - Support BOOT function, BOOT unit can be set from 0-4K
  - Support hardware CRC verification FLASH spatial encoding
  - Support FLASH partition protection (min. unit of 2K)
- **System clock**
  - High speed internal clock: 48MHz/64MHz (HSI)
  - Low speed internal clock: 40KHz (LSI)
- **GPIO (max. 24 I/Os)**
- **LVR(1.9V/2.1V/2.6V)**
- **LVD(2.0V/2.2V/2.4V/2.7V/3.0V/3.7V)**
- **System timer**
  - 24-bit SysTick timer
  - Watchdog timer (WDT)
  - Windowed watchdog timer (WWDT)
- **Normal/sleep/deep sleep/stop mode**
- **Cyclic Redundancy Check (CRC)**
- **Timer(32bit/16bit-TIMER0/1)**
- **Capture, Compare and PWM(CCP0/1)**
  - Support 4-channel concurrent capture, can connect to Hall-effect sensor interface
- **Communication interface**
  - 1 I^2C module (max. speed of 1Mb/s)
  - 1 SSP/SPI module (4 to 16-bit data format adjustable)
  - Max. 2 UART：UART0/1(total 32 receive/transmit FIFO) (TXD1 and RXD1 of UART1 can be set to any interfaces)
- **Serial Wire Debug (2 Wire)**
- **96-bit unique ID(UID)**
- **128-bit user UID(USRUID)**
  - User can set and encrypt (can be use as security key)
- **Enhanced PWM(EPWM)**
  - 6 channels and channels can remap
  - Support individual/complementary/synchronized/grouped output mode
  - Support edge/center aligned mode
  - Support single/continuous/interval update mode
  - Support complementary pwm with dead-time insertion
  - Support mask and pre-set mask (total of 8 mask state cache)
  - Support Hall-effect sensor port (hardware controls PWM output)
  - Support hardware brake and 6 sources of brake signal
- **ADC0(12bit,100Ksps)**
  - Max. 24 input channels
  - Each converting channel has separated product registers
  - Support single/continuous mode
  - Support 2 hardware triggers with 7 sources of trigger
  - 1 converted output comparator, can generate interrupt
- **ADC1(12-bit,1.2Msps)**
  - Max. 24 input channels
  - Each converting channel has separated product registers
  - Support single/continuous/inserting mode
  - Support external trigger mode
  - 1 converted output comparator, can generate interrupt
- **Analog comparator (ACMP0/1)**
  - 4 choices from positive end, negative end can choose internal 1.2V/VDD
  - Support hysteresis voltage choice：10mV/20mV/60mV
  - Support comparator output triggered EPWM brake
- **Programmable gain amplifier (PGA0/1)**
  - 4 choices in positive end
  - Output can connect to internal ADC channel and the input of analog comparator
  - Internal gain of ：4~32
- **Operational amplifier (OP0/1)**
  - Input can connect to internal 1.2V
  - Output can connect to internal ADC channel and the input of analog comparator
  - Can set to comparator mode
- **Support security-related applications and functions**
  - Satisfy IEC60730 CLASS B

1.2 Product Comparison

Product / Peripherals		CMS32M5510	CMS32M5512	CMS32M5524	CMS32M5526	CMS32M5533	CMS32M5536
Supply power of built-in driver		-	5~18V	16~30V	9~36V	5.5~18V	8~20V
Gate Driver		-	3P+3N	3P+3N	3P+3N	6N	6N
Integrated MOS		N	Y	N	N	N	N
Maximum power supply for driver		-	20V	30V	40V	20V	25V
Maximum high side floating VB voltage		-	-	-	-	90V	225V
MCU working voltage		2.1V~5.5V					
Max. clock frequency		64MHz					
Memory	APROM	28/30/31/32KB(1)					
	BOOT	0/1/2/4KB(1)					
	Data Flash	1KB					
	SRAM	8KB					
Timer	SysTick	1 (24-bit)					
	WDT	1					
	WWDT	1					
	TIMER0/1	2 (16/32-bit)					
Enhanced digital peripherals	CRC	CRC-16-CCITT					
	divider	32 / 32 bit					
	CCP	2					
	EPWM	6(16-bit)					
Communi-cation interfaces	UART	2					
	I2C	1					
	SSP/SPI	1					
Analog module	12bit-ADC0 (no. external channels)	22	22	7, 14	13, 23	24	24
	12bit-ADC1 (no. external channels)	22	22	7, 14	13, 23	24	24
	ACMP	2 (2)	2	1	1(4), 2	2	2
	OP	2	2	1 (3), 2	2	2	2
	PGA	2	2	2 (2)	1(4), 2	2	2
GPIOs		22	22	7, 14	13, 23	24	24
LVR		1.9V/2.1V/2.6V					
LVD		2.0V/2.2V/2.4V/2.7V/3.0V/3.7V					
Working temperature		-40~105 ℃					
Packaging		SSOP24	QFN40	SOP16 SSOP24	SSOP24 TSSOP24 QFN40	QFN40 LQFP48	LQFP48

Note:

1) Set the APROM and BOOT space size by system configuration register, APROM and BOOT have max. space 32K.
2) Indicates number of analog modules, analog function is not achieved via pin's I/O, which subject to actual product.
3) Indicates SOP16 packaging has OP module 1.
4) Indicates the number of CMS32M5526S024/CMS32M5526TS024 comparator/PGA is 1.

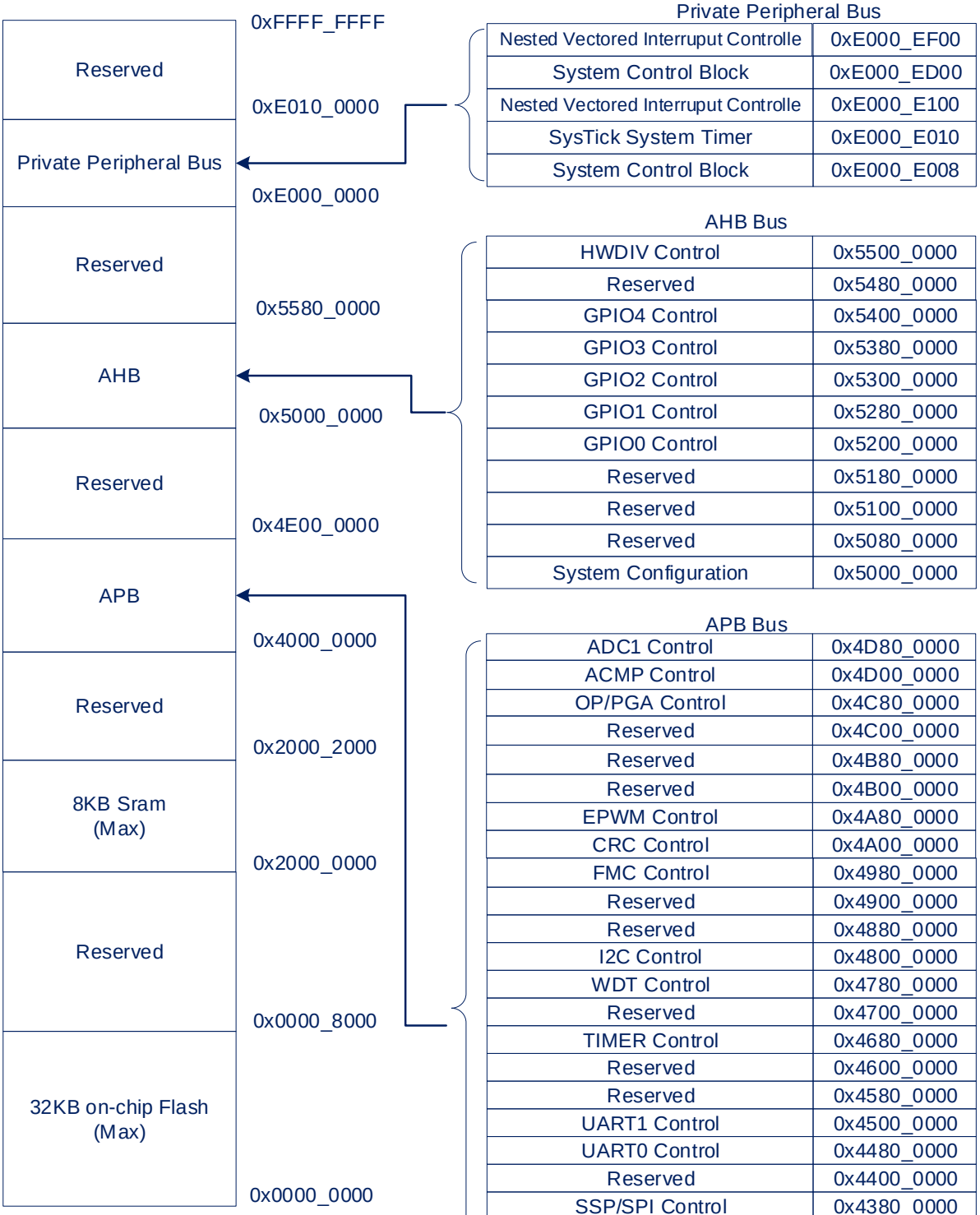
2. System Description

2.1 System Introduction

This series of products has integrated ARM® Cortex®-M0 with Nested Vectored Interrupt Controller. It has parallel I/O interface (support normal input, pull up/down input, push-pull output, leakage opening output and can configure edge/level triggered interrupt), timer (6-bit windowed watchdog timer, 32-bit watchdog timer, 2 programmable timer), SPI, I2C, UART, PWM, CCP, ADC, ACMP, OPA, PGA and other devices. Their main features are as follows:

- Max. 32KB FLASH memory space, max. 8KB SRAM memory,1KB FLASH data space.
- Support BOOT and separated write-protection of programs, support hardware CRC verification of FLASH spatial code, register protection with user-defined ID, hence it is more secure.
- Provide choice of normal mode, sleep mode, deep sleep mode, stop mode. It is more convenient and less power consuming.
- Contain 32-bit hardware divider and 32-bit single period hardware multiplier to achieve faster calculation
- Can configure any I/O interface as serial transmit/receive interface meanwhile, it can configure any I/O interface as input interface of ADC. Therefore, it is more convenient.
- Contains enhanced PWM with dead-time insertion, duty cycle interval update and individual/ complementary/ synchronized output.
- Contains strong analog IP such as 12-bit ADC with max. 1.2Msps, support analog comparator with choice hysteresis, programmable gain amplifier with adjustable gain and operational amplifier.

2.2 Register Map



Private Peripheral Bus

Nested Vectored Interruput Controlle	0xE000_EF00
System Control Block	0xE000_ED00
Nested Vectored Interruput Controlle	0xE000_E100
SysTick System Timer	0xE000_E010
System Control Block	0xE000_E008

AHB Bus

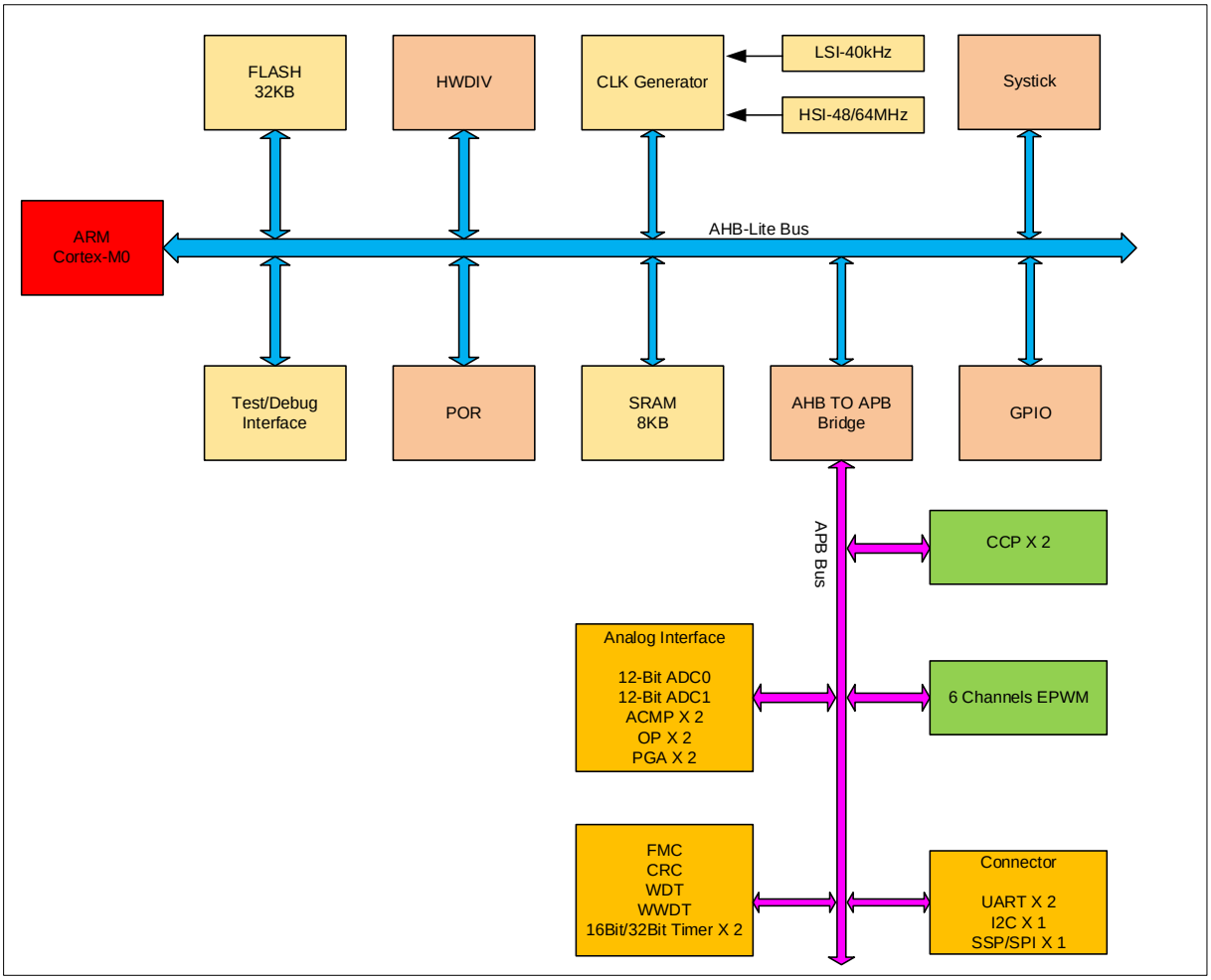
HWDIV Control	0x5500_0000
Reserved	0x5480_0000
GPIO4 Control	0x5400_0000
GPIO3 Control	0x5380_0000
GPIO2 Control	0x5300_0000
GPIO1 Control	0x5280_0000
GPIO0 Control	0x5200_0000
Reserved	0x5180_0000
Reserved	0x5100_0000
Reserved	0x5080_0000
System Configuration	0x5000_0000

APB Bus

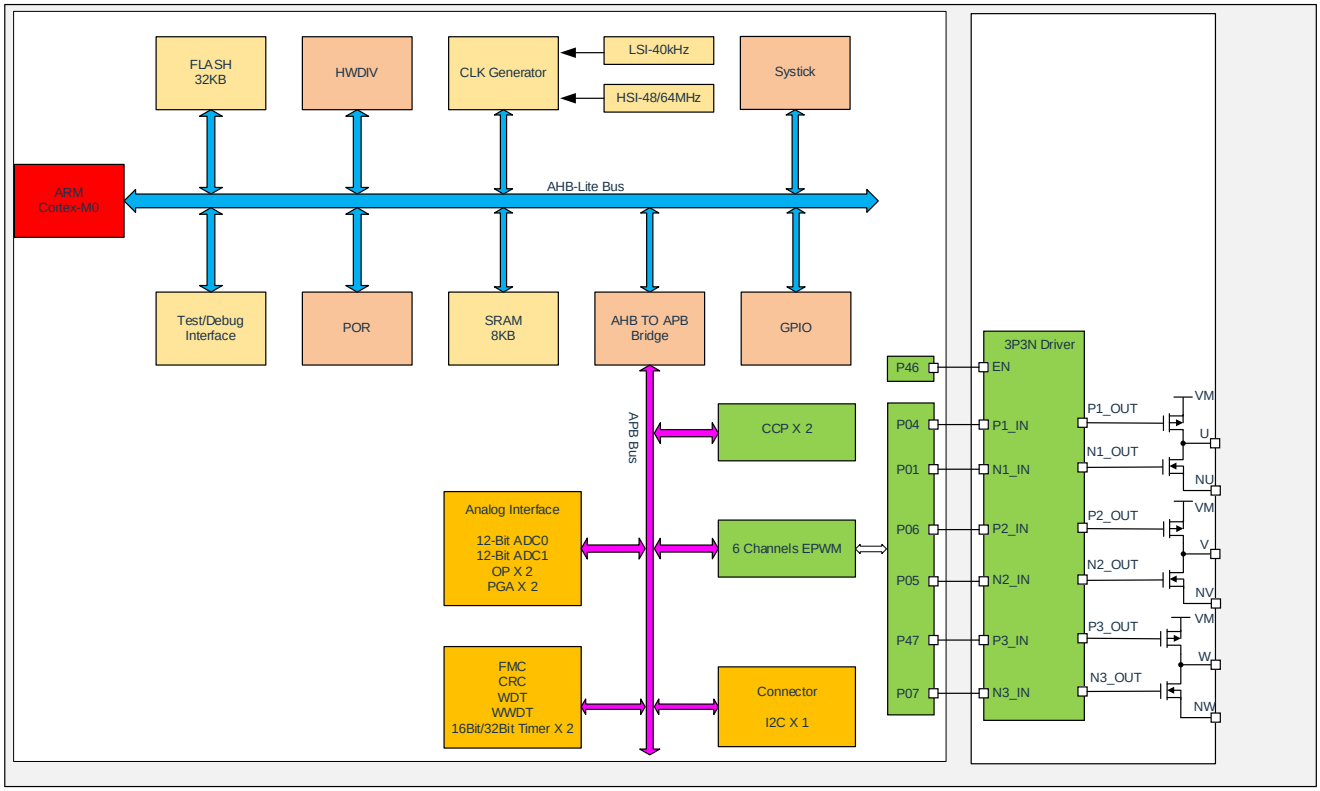
ADC1 Control	0x4D80_0000
ACMP Control	0x4D00_0000
OP/PGA Control	0x4C80_0000
Reserved	0x4C00_0000
Reserved	0x4B80_0000
Reserved	0x4B00_0000
EPWM Control	0x4A80_0000
CRC Control	0x4A00_0000
FMC Control	0x4980_0000
Reserved	0x4900_0000
Reserved	0x4880_0000
I2C Control	0x4800_0000
WDT Control	0x4780_0000
Reserved	0x4700_0000
TIMER Control	0x4680_0000
Reserved	0x4600_0000
Reserved	0x4580_0000
UART1 Control	0x4500_0000
UART0 Control	0x4480_0000
Reserved	0x4400_0000
SSP/SPI Control	0x4380_0000
CCP Control	0x4280_0000
Reserved	0x4200_0000
WWDT Control	0x4180_0000
Reserved	0x4100_0000
Reserved	0x4080_0000
Reserved	0x4000_0000

2.3 System Structure

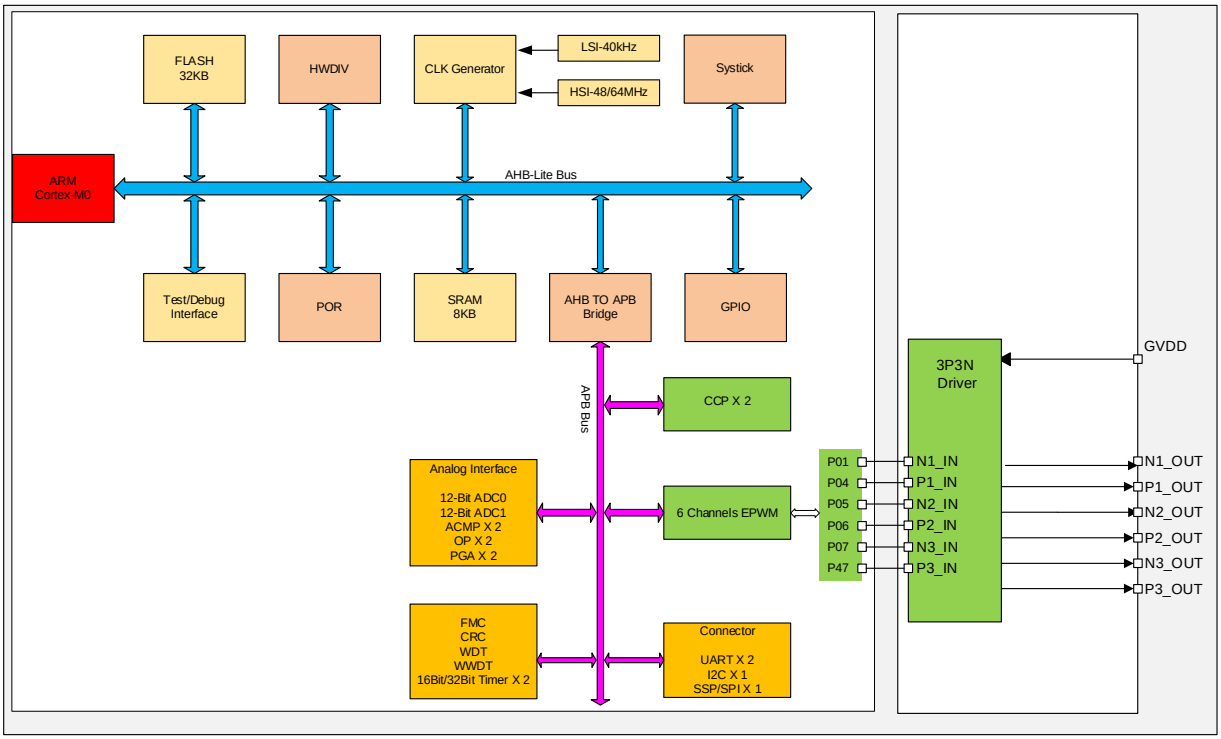
2.3.1 CMS32M5510



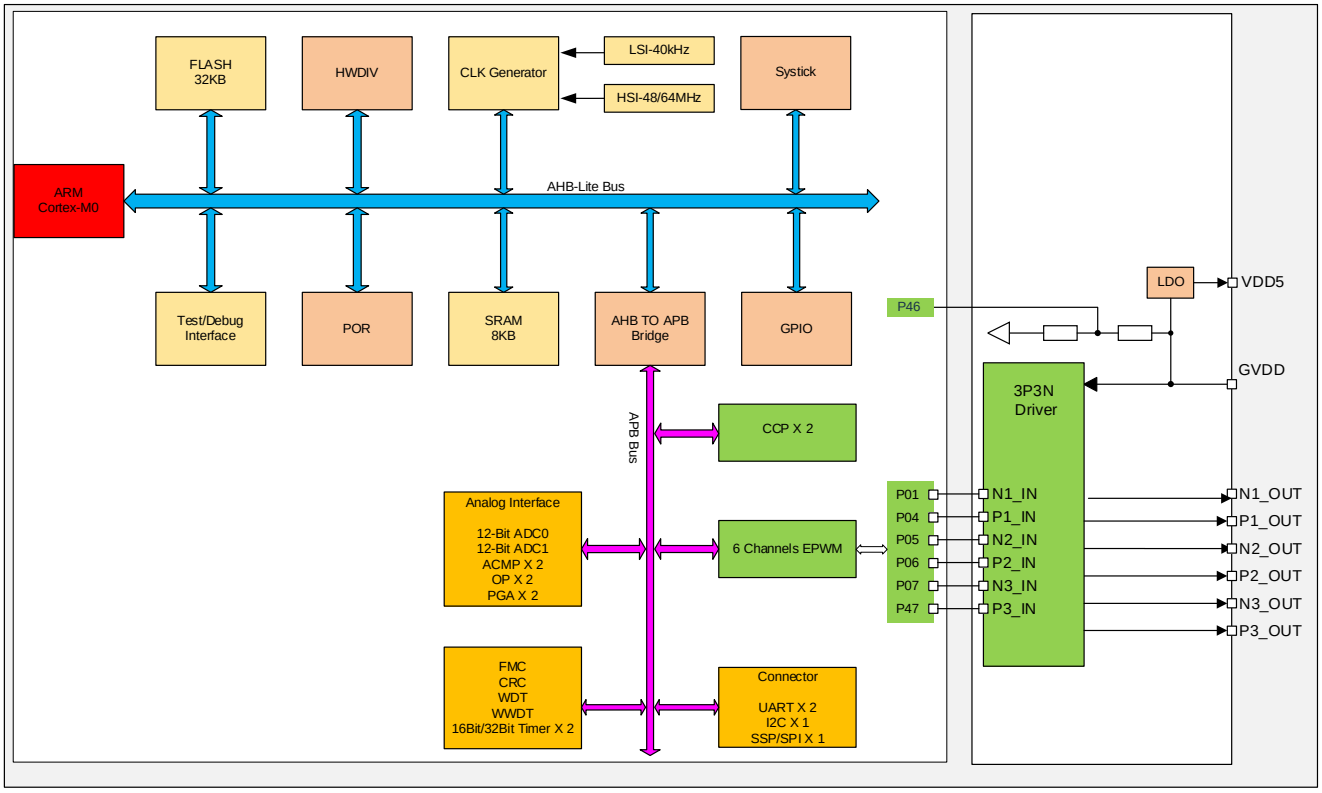
2.3.2 CMS32M5512



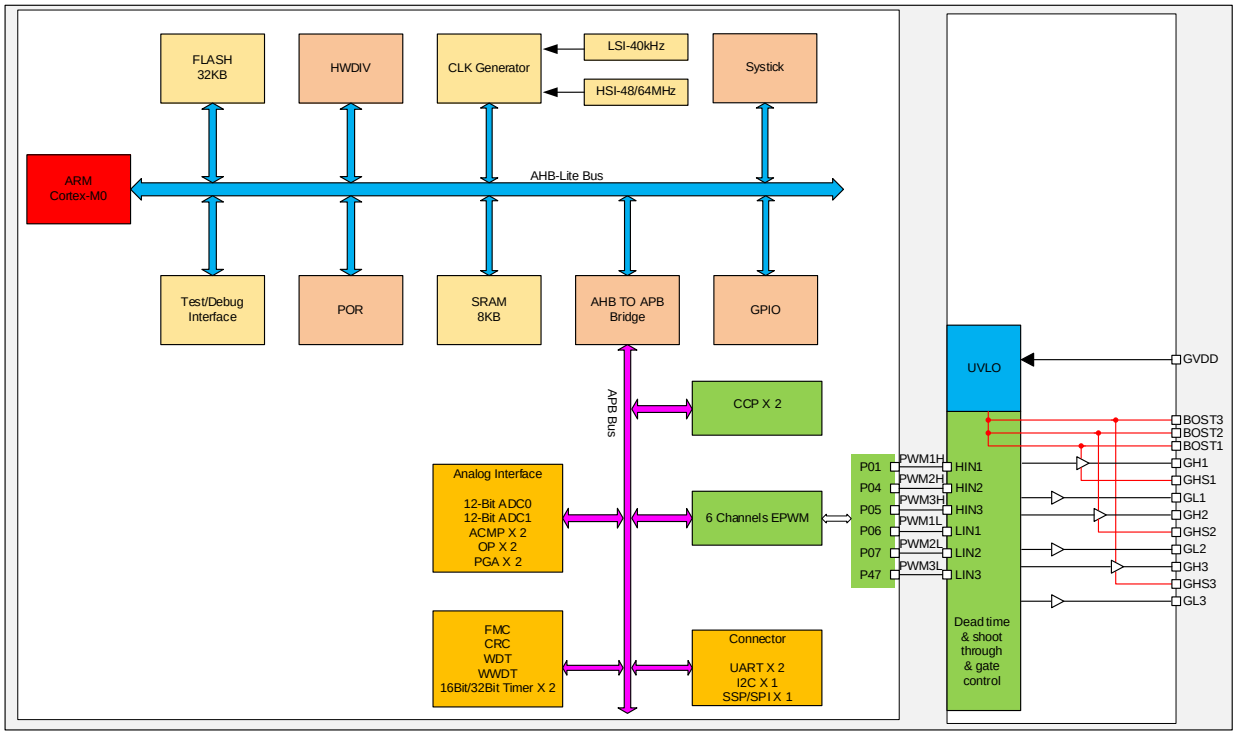
2.3.3 CMS32M5524



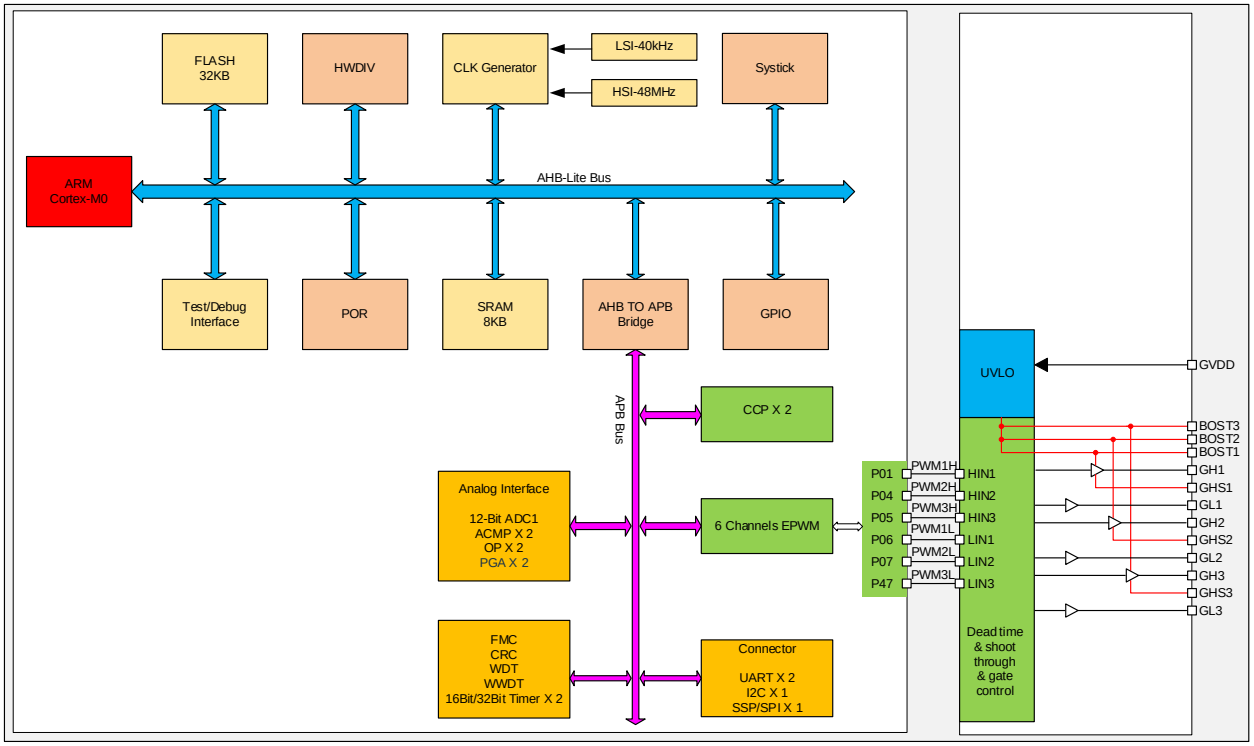
2.3.4 CMS32M5526



2.3.5 CMS32M5533



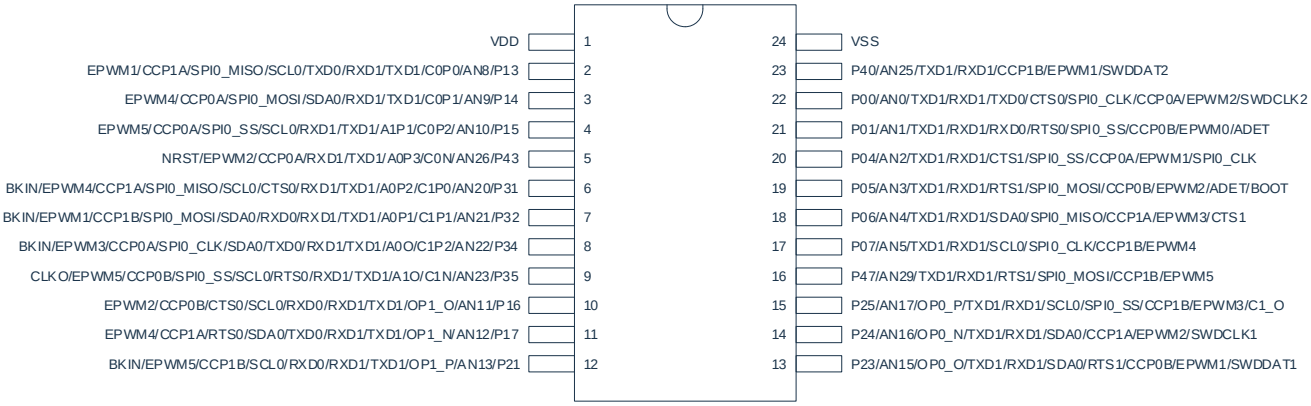
2.3.6 CMS32M5536



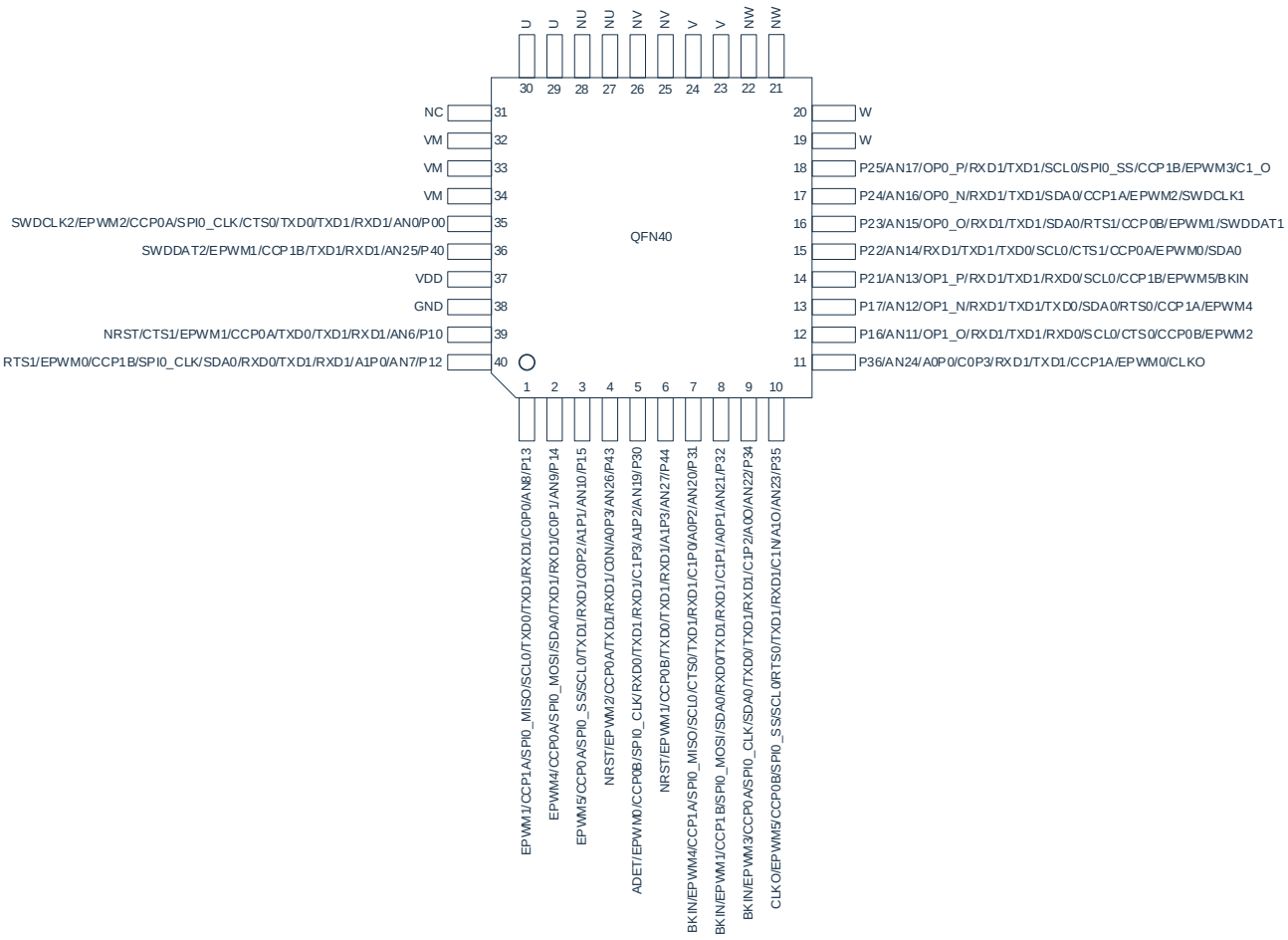
3. Pin Configuration

3.1 Pin Description

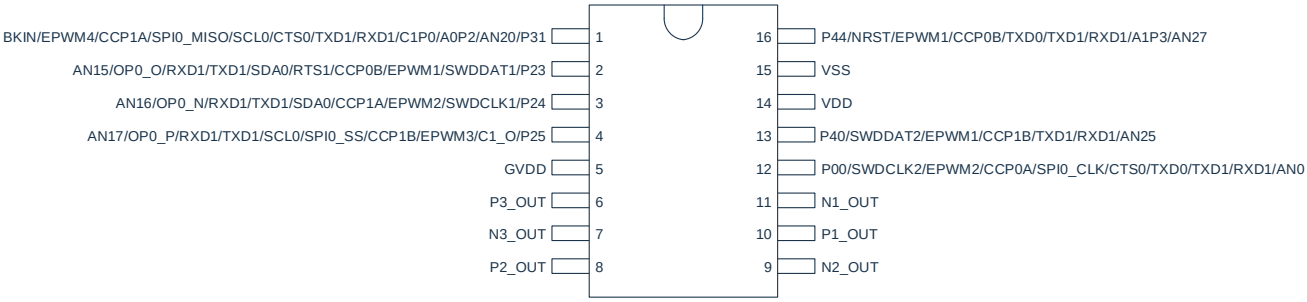
3.1.1 CMS32M5510(SSOP24)



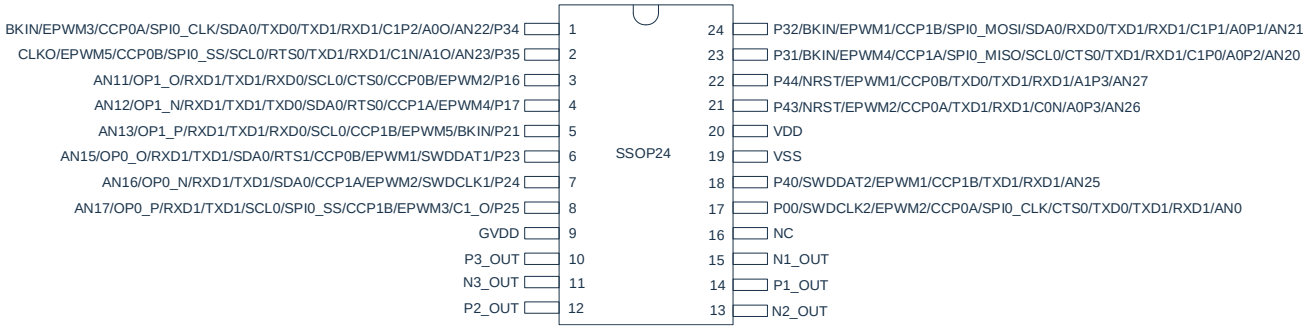
3.1.2 CMS32M5512(QFN40)



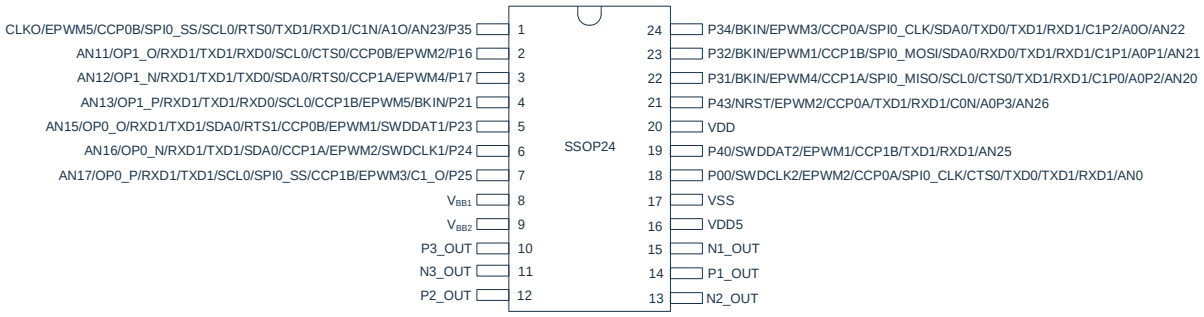
3.1.3 CMS32M5524(SOP16)



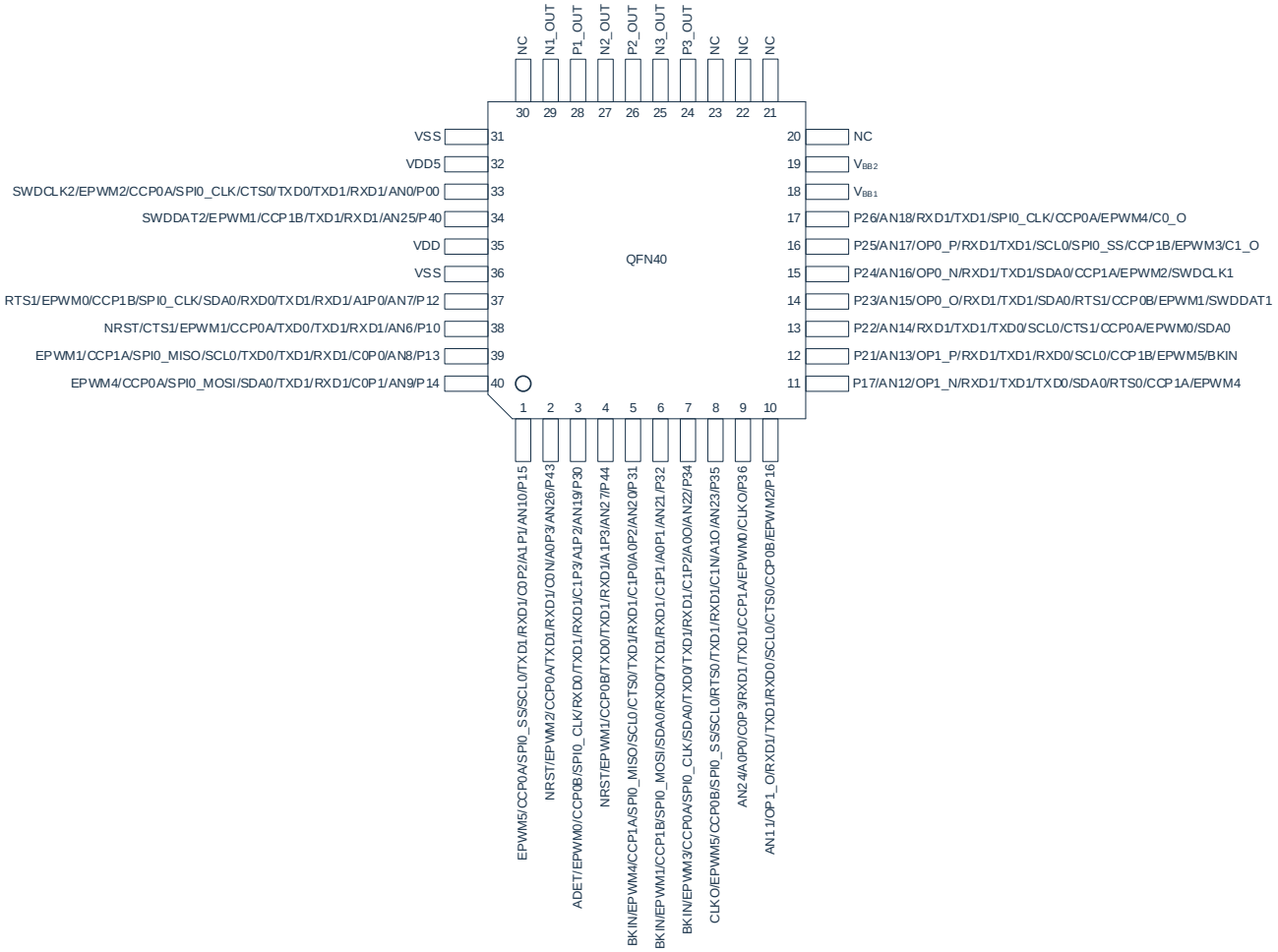
3.1.4 CMS32M5524(SSOP24)



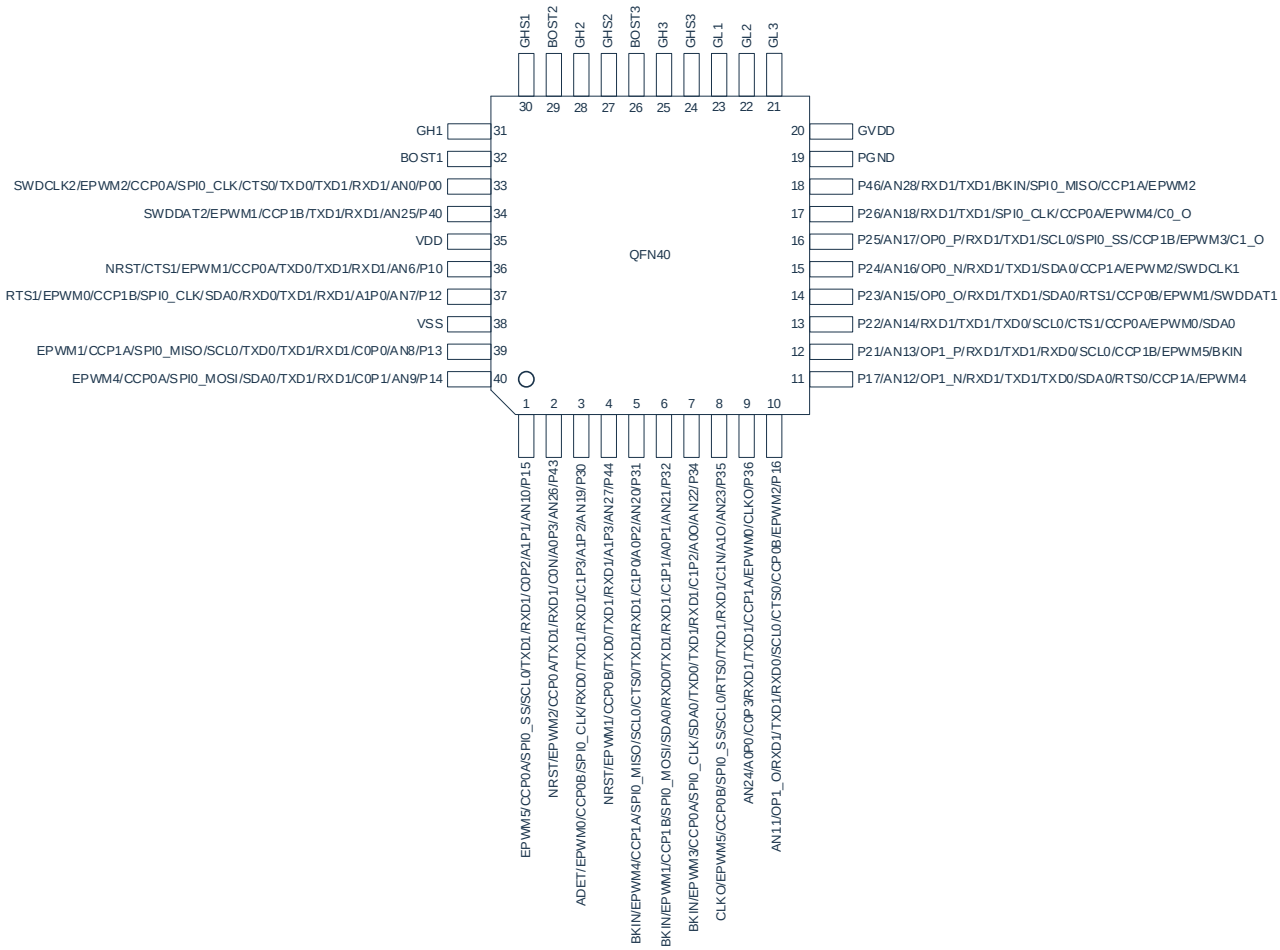
3.1.5 CMS32M5526(SSOP24/TSSOP24)



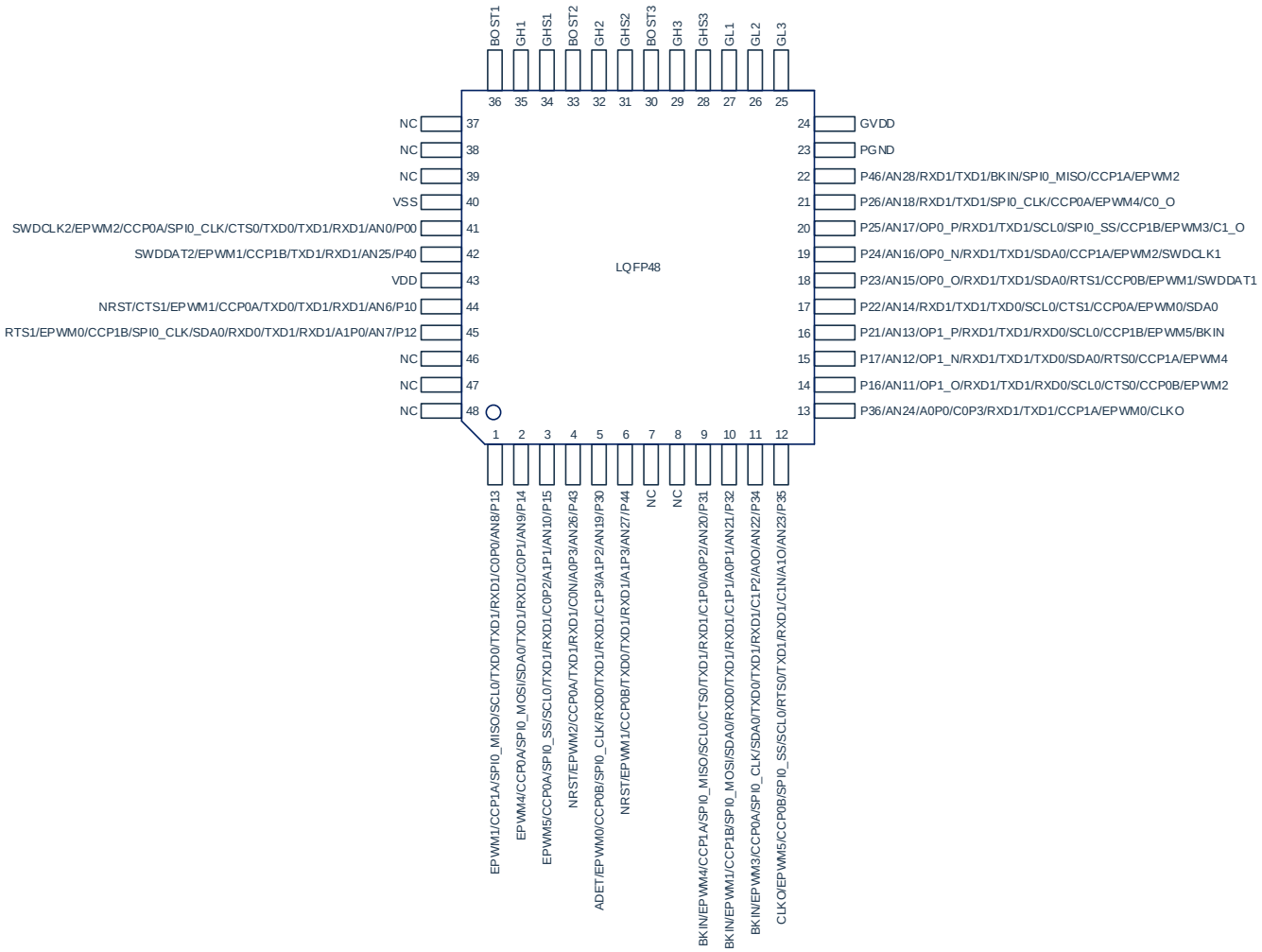
3.1.6 CMS32M5526(QFN40)



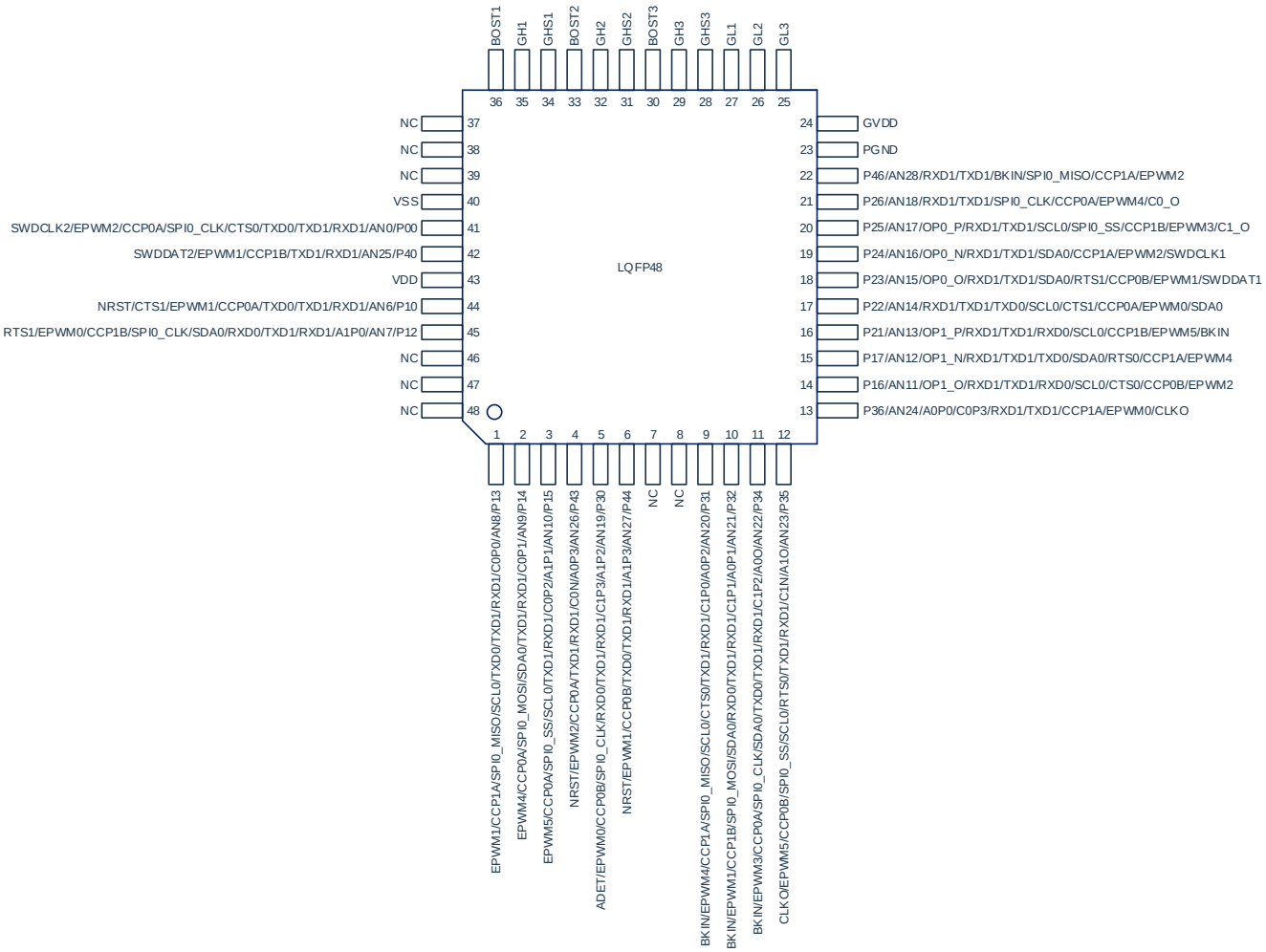
3.1.7 CMS32M5533(QFN40)



3.1.8 CMS32M5533(LQFP48)



3.1.9 CMS32M5536(LQFP48)



3.2 Pin functions Description

Pin name	Symbol description
I/O	Digital input/output.
I	Digital input.
O	Digital output.
AI	Analog input.
AO	Analog output.
P	GND OR VDD

3.2.1 CMS32M5510/12/24/26 Function description

Pin number						pin name	pin type	description
5510	5512	5524		5526				
SSOP 24	QFN 40	SOP 16	SSOP 24	SSOP24/ TSSOP 24	QFN 40			
2	1	-	-	-	39	P13	I/O	General input/output pin
						AN8	AI	ADC analog input pin 8
						C0P0	AI	ACMP0 positive input channel 0
						ECAP00	I	ACMP0 positive input channel 0 as input capture
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						TXD0	O	UART0 data output pin
						SCL0	I/O	I2C0 clock input/output pin
						SPI0_MISO	I/O	SPI0 master input/ slave output pin
						CCP1A	I/O	CCP1 input capture/ PWM output A pin
						EPWM1	O	EPWM output channel1
3	2	-	-	-	40	P14	I/O	General input/output pin
						AN9	AI	ADC analog input pin
						C0P1	AI	ACMP0 positive input channel 1
						ECAP01	I	ACMP0 positive input channel1 as input capture
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						SDA0	I/O	I2C0 data input/output pin
						SPI0_MOSI	I/O	SPI0 master output/slave input pin
						CCP0A	I/O	CCP0 input capture/PWM output A pin
						EPWM4	O	EPWM output channel 4
4	3	-	-	-	1	P15	I/O	General input/output pin
						AN10	AI	ADC analog input channel 10
						C0P2	AI	ACMP0 positive input channel 2
						ECAP02	I	ACMP0 positive input channel 2 as input capture
						A1P1	AI	PAG1 positive input channel 1
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						SCL0	I/O	I2C0 clock input/output pin
						SPI0_SS	I/O	SPI0 slave select pin
						CCP0A	I/O	CCP0 input capture/PWM output A pin

Pin number						pin name	pin type	description
5510	5512	5524		5526				
SSOP 24	QFN 40	SOP 16	SSOP 24	SSOP24/ TSSOP 24	QFN 40			
						EPWM5	O	EPWM output channel 5
5	4	-	21	21	2	P43	I/O	General input/output pin
						AN26	AI	ADC analog input channel 26
						C0N	AI	ACMP0 negative input channel
						A0P3	AI	PAG0 positive input channel 3
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						NRST	I	External reset pin
						CCP0A	I/O	CCP0 input capture/PWM output A pin
						EPWM2	O	EPWM output channel2
-	5	-	-	-	3	P30	I/O	General input/output pin
						AN19	AI	ADC analog input channel 19
						C1P3	AI	ACMP1 positive input channel 3
						ECAP13	I	ACMP1 positive input channel 3 as input capture
						A1P2	AI	PAG1 positive input channel 2
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						RXD0	I	UART0 data input pin
						SPI0_CLK	I/O	SPI0 clock input/output pin
						CCP0B	I/O	CCP0 input capture/PWM output B pin
						EPWM0	O	EPWM outputchannel0
						ADET	I	ADC external enabled digital input
-	6	16	22	-	4	P44	I/O	general input/output pin
						AN27	AI	ADC analog input channel 27
						A1P3	AI	PAG1 positive input channel 3
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						NRST	I	External reset pin
						TXD0	O	UART0 data output pin
						CCP0B	I/O	CCP0 input capture/ PWM output B pin
						EPWM1	O	EPWM outputchannel1
-	31	-	16	-	20,21 ,22, 23,30	NC	-	Not connected
6	7	1	23	22	5	P31	I/O	General input/output pin
						AN20	AI	ADC analog input channel 20
						C1P0	AI	ACMP1 positive input channel 0
						ECAP10	I	ACMP1 positive input channel 0 as input capture
						A0P2	AI	PAG0 positive input channel 2
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						CTS0	I	UART0 clear to send pin
						SCL0	I/O	I2C0 clock input/output pin
						SPI0_MISO	I/O	SPI0 master input/slave output pin
						CCP1A	I/O	CCP input capture/PWM0output A pin

Pin number						pin name	pin type	description
5510	5512	5524		5526				
SSOP 24	QFN 40	SOP 16	SSOP 24	SSOP24/ TSSOP 24	QFN 40			
						BKIN	I	EPWM brake input
						EPWM4	O	EPWM outputchannel4
7	8	-	24	23	6	P32	I/O	General input/output pin
						AN21	AI	ADC analog input channel 21
						C1P1	AI	ACMP1 positive input channel 1
						ECAP11	I	ACMP1 positive input channel1 as input capture
						A0P1	AI	PAG0 positive input channel 1
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						RXD0	I	UART0 data input pin
						SDA0	I/O	I2C0 data input/output pin
						SPI0_MOSI	I/O	SPI0 master output/slave input pin
						CCP1B	I/O	CCP1 input capture/PWM output B pin
						BKIN	I	EPWM brake input
						EPWM1	O	EPWM output channel 1
8	9	-	1	24	7	P34	I/O	General input/output pin
						AN22	AI	ADC analog input channel 22
						C1P2	AI	ACMP1 positive input channel 2
						ECAP12	I	ACMP1 positive input channel 2as input capture
						A0O	AO	PAG0 output channel
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						TXD0	O	UART0 data output pin
						SDA0	I/O	I2C0 data input/output pin
						SPI0_CLK	I/O	SPI0 clock input/output pin
						CCP0A	I/O	CCP0 input capture/PWM output A pin
						BKIN	I	EPWM brake input
						EPWM3	O	EPWM output channel 3
9	10	-	2	1	8	P35	I/O	General input/output pin
						AN23	AI	ADC analog channel23
						C1N	AI	ACMP1 negative input channel
						A1O	AO	PAG1 output channel
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						RTS0	O	UART0 request to send pin
						SCL0	I/O	SPI0 clock input/output pin
						SPI0_SS	I/O	SPI0 slave select pin
						CCP0B	I/O	CCP0 input capture/PWM output B pin
						EPWM5	O	EPWM output channel 5
						CLKO	O	System clock output pin
-	11	-	-	-	9	P36	I/O	General input/output pin
						AN24	AI	ADC analog channel 23
						C0P3	AI	ACMP0 positive input channel 3
						ECAP03	I	ACMP0 positive input channel 3as input capture

Pin number						pin name	pin type	description
5510	5512	5524		5526				
SSOP 24	QFN 40	SOP 16	SSOP 24	SSOP24/ TSSOP 24	QFN 40			
						A0P0	AI	PAG0 positive input channel 0
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						CCP1A	I/O	CCP1 input capture/PWM output A pin
						EPWM0	O	EPWM output channel 0
						CLKO	O	System clock output pin
10	12	-	3	2	10	P16	I/O	General input/output pin
						AN11	AI	ADC analog channel11
						OP1_O	AO	OPA1 output channel
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						RXD0	I	UART0 data input pin
						SCL0	I/O	I2C0 clock input/output pin
						CTS0	I	UART0 clear to send pin
						CCP0B	I/O	CCP0 input capture/PWM output B pin
						EPWM2	O	EPWM output channel2
11	13	-	4	3	11	P17	I/O	General input/output pin
						AN12	AI	ADC analog channel12
						OP1_N	AI	OPA1 negative input
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						TXD0	O	UART0 data output pin
						SDA0	I/O	I2C0 data input/output pin
						RTS0	O	UART0 request to send pin
						CCP1A	I/O	CCP1 input capture/PWM output A pin
						EPWM4	O	EPWM output channel4
12	14	-	5	4	12	P21	I/O	General input/output pin
						AN13	AI	ADC analog channel13
						OP1_P	AI	OPA1 positive input
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						RXD0	I	UART0 data input pin
						SCL0	I/O	I2C0 clock input/output pin
						CCP1B	I/O	CCP1 input capture/PWM output B pin
						BKIN	I	EPWM brake input
						EPWM5	O	EPWM output channel5
-	15	-	-	-	13	P22	I/O	general input/output pin
						AN14	AI	ADC analog channel 14
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						TXD0	O	UART0 data output pin
						SCL0	I/O	I2C0 clock input/output pin
						CTS1	I	UART0 clear to send pin
						CCP0A	I/O	CCP0 input capture/PWM output A pin
						EPWM0	O	EPWM output channel 0

Pin number						pin name	pin type	description
5510	5512	5524		5526				
SSOP 24	QFN 40	SOP 16	SSOP 24	SSOP24/ TSSOP 24	QFN 40			
						SDA0	I/O	I2C0 data input/output pin
13	16	2	6	5	14	P23	I/O	General input/output pin
						AN15	AI	ADC analog channel15
						OP0_O	AO	OPA0 output channel
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						SDA0	I/O	I2C0 data input/output pin
						RTS1	O	UART1 request to send pin
						CCP0B	I/O	CCP0 input capture/PWM output B pin
						EPWM1	O	EPWM output channel1
						SWDDAT1	I/O	SWD programming, debugging data input/output pin1
14	17	3	7	6	15	P24	I/O	General input/output pin
						AN16	AI	ADC analog channel16
						OP0_N	AI	OPA0 negative input channel
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						SDA0	I/O	I2C0 data input/output pin
						CCP1A	I/O	CCP1 input capture/PWM output A pin
						EPWM2	O	EPWM output channel2
						SWDCLK1	I	SWD programming, debugging clock input pin1
15	18	4	8	7	16	P25	I/O	General input/output pin
						AN17	AI	ADC analog channel17
						OP0_P	AI	OPA0 positive input channel
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						SCL0	I/O	I2C0 clock input/output pin
						SPI0_SS	I/O	SPI0 slave select pin
						CCP1B	I/O	CCP1 input capture/PWM output B pin
						EPWM3	O	EPWM output channel3
						C1_O	O	ACMP1 output channel
-	-	-	-	-	17	P26	I/O	General input/output pin
						AN18	AI	ADC analog channel 18
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						SPI0_CLK	I/O	SPI0 clock input/output pin
						CCP0A	I/O	CCP0 input capture/PWM output A pin
						EPWM4	O	EPWM output channel 4
						C0_O	O	ACMP0 output channel
-	-	5	9	-	-	GVDD	P	Internal generated power supply pin
-	-	-	-	8	18	V_{BB1}	P	5V power supply terminal
-	-	-	-	9	19	V_{BB2}	P	Drive power supply terminal
-	19,20	-	-	-	-	W	O	W phase output
-	21,22	-	-	-	-	NW	O	W-phase low-side N power tube source pole
-	23,24	-	-	-	-	V	O	V phase output

Pin number						pin name	pin type	description
5510	5512	5524		5526				
SSOP 24	QFN 40	SOP 16	SSOP 24	SSOP24/ TSSOP 24	QFN 40			
-	25,26	-	-	-	-	NV	O	V-phase low-side N power tube source pole
-	27,28	-	-	-	-	NU	O	U-phase low-side N power tube source pole
-	29,30	-	-	-	-	U	O	U phase output
-	32,33 ,34	-	-	-	-	VM	P	Power side
24	38	15	19	17	31,36	VSS/GND	P	Voltage source supply(ground)
22	35	12	17	18	33	P00	I/O	General input/output pin
						AN0	AI	ADC analog channel 0
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						TXD0	O	UART0 transmit data output pin
						CTS0	I	UART0 clear to send pin
						SPI0_CLK	I/O	SPI0 clock input/output pin
						CCP0A	I/O	PWM0 input capture/PWM output A pin
						EPWM2	O	EPWM output channel2
						SWDCLK2	I	SWD programming, debugging clock input pin2
23	36	13	18	19	34	P40	I/O	General input/output pin
						AN25	AI	ADC analog input channel 25
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						CCP1B	I/O	CCP1 input capture/PWM output B pin
						EPWM1	O	EPWM output channel1
						SWDDAT2	I/O	SWD programming, debugging data input/output pin2
1	37	14	20	20	35	VDD	P	Power supply
-	-	-	-	16	32	VDD5	P	5V Poweroutput
-	39	-	-	-	38	P10	I/O	General input/output pin
						AN6	AI	ADC analog input channel 6
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						TXD0	O	UART0 data output pin
						NRST	I	External reset pin
						CCP0A	I/O	CCP0 input capture/PWM output A pin
						EPWM1	O	EPWM output channel1
						CTS1	I	UART1 clear to send pin
-	40		-	-	37	P12	I/O	General input/output pin
						AN7	AI	ADC analog input pin7
						A1P0	AI	PAG1 positive input channel 0
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						RXD0	I	UART0 data input pin
						SDA0	I/O	I2C0 data input/output pin
						SPI0_CLK	I/O	SPI0 clock input/output pin
						CCP1B	I/O	CCP1 input capture/PWM output B pin
						EPWM0	O	EPWM output channel 0

Pin number						pin name	pin type	description
5510	5512	5524		5526				
SSOP 24	QFN 40	SOP 16	SSOP 24	SSOP24/ TSSOP 24	QFN 40			
						RTS1	O	UART1 request to send pin
-	-	6	10	10	24	P3_OUT	O	P3 output signal
-	-	7	11	11	25	N3_OUT	O	N3 output signal
-	-	8	12	12	26	P2_OUT	O	P2 output signal
-	-	9	13	13	27	N2_OUT	O	N2 output signal
-	-	10	14	14	28	P1_OUT	O	P1 output signal
-	-	11	15	15	29	N1_OUT	O	N1 output signal
21	-	-	-	-	-	P01	I/O	General input/output pin
						AN1	AI	ADC analog channel 1
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						RXD0	I	UART0 data input pin
						RTS0	O	UART0 request to send pin
						SPI0_SS	I/O	SPI0 salve select pin
						CCP0B	I/O	CCP0 input capture/PWM output B pin
						EPWM0	O	EPWM output channel 0
						ADET	I	ADC external enable digital input
20	-	-	-	-	-	P04	I/O	General input/output pin
						AN2	AI	ADC analog channel 2
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						CTS1	I	UART1 request to send pin
						SPI0_SS	I/O	SPI0 salve select pin
						CCP0A	I/O	CCP0 input capture/PWM output B pin
						EPWM1	O	EPWM output channel 1
						SPI0_CLK	I/O	SPI0 clock input/output pin
19	-	-	-	-	-	P05	I/O	General input/output pin
						AN3	AI	ADC analog channel 3
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						RTS1	O	UART1 request to send pin
						SPI0_MOSI	I/O	SPI0 master input/slave output pin
						CCP0B	I/O	CCP0 input capture/PWM output B pin
						EPWM2	O	EPWM output channel 2f
						BOOT	I	BOOT configuration input pin
						ADET	I	ADC external enable digital input
18	-	-	-	-	-	P06	I/O	General input/output pin
						AN4	AI	ADC analog channel 4
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						SDA0	I/O	I2C0 data input/output pin
						SPI0_MISO	I/O	SPI0 master input/slave output pin
						CCP1A	I/O	CCP1 input capture/PWM output A pin
						EPWM3	O	EPWM output channel 1
						CTS1	I	UART1 request to send pin

Pin number						pin name	pin type	description
5510	5512	5524		5526				
SSOP 24	QFN 40	SOP 16	SSOP 24	SSOP24/ TSSOP 24	QFN 40			
17	-	-	-	-	-	P07	I/O	General input/output pin
						AN5	AI	ADC analog channel 5
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						SCL0	I/O	I2C0 clock input/output pin
						SPI0_CLK	I/O	SPI0 clock input/output pin
						CCP1B	I/O	CCP1 input capture/PWM output B pin
						EPWM4	O	EPWM output channel 4
16	-	-	-	-	-	P47	I/O	General input/output pin
						AN29	AI	ADC analog output 28
						TXD1	O	UART1 data output pin
						RXD1	I	UART1 data input pin
						RTS1	O	UART1 request to send pin
						SPI0_MOSI	I/O	SPI0 master input/slave output pin
						CCP1B	I/O	CCP1 input capture/PWM output B pin
						EPWM5	O	EPWM output channel 5

3.2.2 CMS32M5533/36 Function description

Pin number			pin name	pin type	description
5533		5536			
LQFP48	QFN40	LQFP48			
1	39	1	P13	I/O	General input/output pin
			AN8	AI	ADC analog input pin 8
			C0P0	AI	ACMP0 positive input channel 0
			ECAP00	I	ACMP0 positive input channel 0 as input capture
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			TXD0	O	UART0 data output pin
			SCL0	I/O	I2C0 clock input/output pin
			SPI0_MISO	I/O	SPI0 master input/ slave output pin
			CCP1A	I/O	CCP1 input capture/ PWM output A pin
			EPWM1	O	EPWM output channel1
2	40	2	P14	I/O	General input/output pin
			AN9	AI	ADC analog input pin
			C0P1	AI	ACMP0 positive input channel 1
			ECAP01	I	ACMP0 positive input channel1 as input capture
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SDA0	I/O	I2C0 data input/output pin
			SPI0_MOSI	I/O	SPI0 master output/slave input pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM4	O	EPWM output channel 4
3	1	3	P15	I/O	General input/output pin
			AN10	AI	ADC analog input channel 10

Pin number			pin name	pin type	description
5533		5536			
LQFP48	QFN40	LQFP48			
			C0P2	AI	ACMP0 positive input channel 2
			ECAP02	I	ACMP0 positive input channel 2 as input capture
			A1P1	AI	PAG1 positive input channel 1
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SCL0	I/O	I2C0 clock input/output pin
			SPI0_SS	I/O	SPI0 slave select pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM5	O	EPWM output channel 5
4	2	4	P43	I/O	General input/output pin
			AN26	AI	ADC analog input channel 26
			C0N	AI	ACMP0 negative input channel
			A0P3	AI	PAG0 positive input channel 3
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			NRST	I	External reset pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM2	O	EPWM output channel2
5	3	5	P30	I/O	General input/output pin
			AN19	AI	ADC analog input channel 19
			C1P3	AI	ACMP1 positive input channel 3
			ECAP13	I	ACMP1 positive input channel 3 as input capture
			A1P2	AI	PAG1 positive input channel 2
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RXD0	I	UART0 data input pin
			SPI0_CLK	I/O	SPI0 clock input/output pin
			CCP0B	I/O	CCP0 input capture/PWM output B pin
			EPWM0	O	EPWM outputchannel0
			ADET	I	ADC external enabled digital input
6	4	6	P44	I/O	general input/output pin
			AN27	AI	ADC analog input channel 27
			A1P3	AI	PAG1 positive input channel 3
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			NRST	I	External reset pin
			TXD0	O	UART0 data output pin
			CCP0B	I/O	CCP0 input capture/ PWM output B pin
			EPWM1	O	EPWM outputchannel1
7,8,37, 38,39, 46,47,4 8	-	7,8,37, 38,39,4 6,47,48	NC	-	Not connected
9	5	9	P31	I/O	General input/output pin
			AN20	AI	ADC analog input channel 20
			C1P0	AI	ACMP1 positive input channel 0
			ECAP10	I	ACMP1 positive input channel 0 as input capture

Pin number			pin name	pin type	description
5533		5536			
LQFP48	QFN40	LQFP48			
			A0P2	AI	PAG0 positive input channel 2
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			CTS0	I	UART0 clear to send pin
			SCL0	I/O	I2C0 clock input/output pin
			SPI0_MISO	I/O	SPI0 master input/slave output pin
			CCP1A	I/O	CCP input capture/PWM0output A pin
			BKIN	I	EPWM brake input
			EPWM4	O	EPWM outputchannel4
10	6	10	P32	I/O	General input/output pin
			AN21	AI	ADC analog input channel 21
			C1P1	AI	ACMP1 positive input channel 1
			ECAP11	I	ACMP1 positive input channel1 as input capture
			A0P1	AI	PAG0 positive input channel 1
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RXD0	I	UART0 data input pin
			SDA0	I/O	I2C0 data input/output pin
			SPI0_MOSI	I/O	SPI0 master output/slave input pin
			CCP1B	I/O	CCP1 input capture/PWM output B pin
			BKIN	I	EPWM brake input
			EPWM1	O	EPWM output channel 1
11	7	11	P34	I/O	General input/output pin
			AN22	AI	ADC analog input channel 22
			C1P2	AI	ACMP1 positive input channel 2
			ECAP12	I	ACMP1 positive input channel 2as input capture
			A0O	AO	PAG0 output channel
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			TXD0	O	UART0 data output pin
			SDA0	I/O	I2C0 data input/output pin
			SPI0_CLK	I/O	SPI0 clock input/output pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			BKIN	I	EPWM brake input
			EPWM3	O	EPWM output channel 3
12	8	12	P35	I/O	General input/output pin
			AN23	AI	ADC analog channel23
			C1N	AI	ACMP1 negative input channel
			A1O	AO	PAG1 output channel
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RTS0	O	UART0 request to send pin
			SCL0	I/O	SPI0 clock input/output pin
			SPI0_SS	I/O	SPI0 slave select pin
			CCP0B	I/O	CCP0 input capture/PWM output B pin
			EPWM5	O	EPWM output channel 5

Pin number			pin name	pin type	description
5533		5536			
LQFP48	QFN40	LQFP48			
			CLKO	O	System clock output pin
13	9	13	P36	I/O	General input/output pin
			AN24	AI	ADC analog channel 23
			C0P3	AI	ACMP0 positive input channel 3
			ECAP03	I	ACMP0 positive input channel 3as input capture
			A0P0	AI	PAG0 positive input channel 0
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			CCP1A	I/O	CCP1 input capture/PWM output A pin
			EPWM0	O	EPWM output channel 0
			CLKO	O	System clock output pin
14	10	14	P16	I/O	General input/output pin
			AN11	AI	ADC analog channel11
			OP1_O	AO	OPA1 output channel
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RXD0	I	UART0 data input pin
			SCL0	I/O	I2C0 clock input/output pin
			CTS0	I	UART0 clear to send pin
			CCP0B	I/O	CCP0 input capture/PWM output B pin
			EPWM2	O	EPWM output channel2
15	11	15	P17	I/O	General input/output pin
			AN12	AI	ADC analog channel12
			OP1_N	AI	OPA1 negative input
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			TXD0	O	UART0 data output pin
			SDA0	I/O	I2C0 data input/output pin
			RTS0	O	UART0 request to send pin
			CCP1A	I/O	CCP1 input capture/PWM output A pin
			EPWM4	O	EPWM output channel4
16	12	16	P21	I/O	General input/output pin
			AN13	AI	ADC analog channel13
			OP1_P	AI	OPA1 positive input
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RXD0	I	UART0 data input pin
			SCL0	I/O	I2C0 clock input/output pin
			CCP1B	I/O	CCP1 input capture/PWM output B pin
			BKIN	I	EPWM brake input
			EPWM5	O	EPWM output channel5
17	13	17	P22	I/O	general input/output pin
			AN14	AI	ADC analog channel 14
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			TXD0	O	UART0 data output pin

Pin number			pin name	pin type	description
5533		5536			
LQFP48	QFN40	LQFP48			
			SCL0	I/O	I2C0 clock input/output pin
			CTS1	I	UART0 clear to send pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM0	O	EPWM output channel 0
			SDA0	I/O	I2C0 data input/output pin
18	14	18	P23	I/O	General input/output pin
			AN15	AI	ADC analog channel15
			OP0_O	AO	OPA0 output channel
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SDA0	I/O	I2C0 data input/output pin
			RTS1	O	UART1 request to send pin
			CCP0B	I/O	CCP0 input capture/PWM output B pin
			EPWM1	O	EPWM output channel1
			SWDDAT1	I/O	SWD programming, debugging data input/output pin1
19	15	19	P24	I/O	General input/output pin
			AN16	AI	ADC analog channel16
			OP0_N	AI	OPA0 negative input channel
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SDA0	I/O	I2C0 data input/output pin
			CCP1A	I/O	CCP1 input capture/PWM output A pin
			EPWM2	O	EPWM output channel2
			SWDCLK1	I	SWD programming, debugging clock input pin1
20	16	20	P25	I/O	General input/output pin
			AN17	AI	ADC analog channel17
			OP0_P	AI	OPA0 positive input channel
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SCL0	I/O	I2C0 clock input/output pin
			SPI0_SS	I/O	SPI0 slave select pin
			CCP1B	I/O	CCP1 input capture/PWM output B pin
			EPWM3	O	EPWM output channel3
			C1_O	O	ACMP1 output channel
21	17	21	P26	I/O	General input/output pin
			AN18	AI	ADC analog channel 18
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			SPI0_CLK	I/O	SPI0 clock input/output pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM4	O	EPWM output channel 4
			C0_O	O	ACMP0 output channel
22	18	22	P46	I/O	General input/output pin
			AN28	AI	ADC analog channel 28
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin

Pin number			pin name	pin type	description
5533		5536			
LQFP48	QFN40	LQFP48			
			SPI0_MISO	I/O	SPI0 master input/slave output pin
			CCP1A	I/O	CCP1 input capture/PWM output A pin
			BKIN	I	EPWM brake input
			EPWM2	O	EPWM output channel2
23	19	23	PGND	P	Internal power ground pin
24	20	24	GVDD	P	Internal generated power supply pin
25	21	25	GL3	O	3 phase low side gate driver output pin
26	22	26	GL2	O	2 phase low side gate driver output pin
27	23	27	GL1	O	1 phase low side gate driver output pin
28	24	28	GHS3	P	3 phase floating high side pin
29	25	29	GH3	O	3 phase high side gate driver output pin
30	26	30	BOST3	P	3 phase high side bootstrap pin
31	27	31	GHS2	P	2 phase high side floating pin
32	28	32	GH2	O	2 phase high side gate driver output pin
33	29	33	BOST2	P	2 phase high side bootstrap pin
34	30	34	GHS1	P	1 phase high side floating pin
35	31	35	GH1	O	1 phase high side gate driver output pin
36	32	36	BOST1	P	1 phase high side bootstrap pin
40	38	40	VSS	P	Voltage source supply(ground)
41	33	41	P00	I/O	General input/output pin
			AN0	AI	ADC analog channel 0
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			TXD0	O	UART0 transmit data output pin
			CTS0	I	UART0 clear to send pin
			SPI0_CLK	I/O	SPI0 clock input/output pin
			CCP0A	I/O	PWM0 input capture/PWM output A pin
			EPWM2	O	EPWM output channel2
			SWDCLK2	I	SWD programming, debugging clock input pin2
42	34	42	P40	I/O	General input/output pin
			AN25	AI	ADC analog input channel 25
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			CCP1B	I/O	CCP1 input capture/PWM output B pin
			EPWM1	O	EPWM output channel1
			SWDDAT2	I/O	SWD programming, debugging data input/output pin2
43	35	43	VDD	P	Power supply
44	36	44	P10	I/O	General input/output pin
			AN6	AI	ADC analog input channel 6
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			TXD0	O	UART0 data output pin
			NRST	I	External reset pin
			CCP0A	I/O	CCP0 input capture/PWM output A pin
			EPWM1	O	EPWM output channel1
			CTS1	I	UART1 clear to send pin

Pin number			pin name	pin type	description
5533		5536			
LQFP48	QFN40	LQFP48			
45	37	45	P12	I/O	General input/output pin
			AN7	AI	ADC analog input pin7
			A1P0	AI	PAG1 positive input channel 0
			TXD1	O	UART1 data output pin
			RXD1	I	UART1 data input pin
			RXD0	I	UART0 data input pin
			SDA0	I/O	I2C0 data input/output pin
			SPI0_CLK	I/O	SPI0 clock input/output pin
			CCP1B	I/O	CCP1 input capture/PWM output B pin
			EPWM0	O	EPWM output channel 0
			RTS1	O	UART1 request to send pin

3.3 GPIO Characteristic

Various function sharing of pin. Each I/O interface can be configured as the corresponding digital or analog function. I/O as a general purpose GPIO interface has the following characteristics:

- It can be configured as normal input, pull-up input, pull-down input, push-pull output, leakage opening output without pull-up.
- Configurable high level, low level, rising edge, falling edge, double edge trigger interrupt.
- Configurable high level, low level, rising edge, falling edge to wake up the chip in sleep/deep sleep/stop mode.
- Configurable tow levels of I/O speed.
- Configurable two levels of output current.

3.4 Pin Function List

Function symbol									
	CONFIG	0	1	2	3	4	5	6	7
P00	-	GPIO	Note(3)	TXD0	CTS0	SPI0_CLK	CCP0A	EPWM2	SWDCLK2(5)
P01	-	GPIO	ANA	RXD0	RTS0	SPI0_SS	CCP0B	EPWM0	ADET
P04	-	GPIO	ANA	-	CTS1	SPI0_SS	CCP0A	EPWM1	SPI0_CLK
P05	BOOT	GPIO	ANA	-	RTS1	SPI0_MOSI	CCP0B	EPWM2	ADET
P06	-	GPIO	ANA	-	SDA0	SPI0_MISO	CCP1A	EPWM3	CTS1
P07	-	GPIO	ANA	-	SCL0	SPI0_CLK	CCP1B	EPWM4	-
P10	NRST	GPIO	ANA	TXD0	-	-	CCP0A	EPWM1	CTS1
P12	-	GPIO	ANA	RXD0	SDA0	SPI0_CLK	CCP1B	EPWM0	RTS1
P13	-	GPIO	ANA	TXD0	SCL0	SPI0_MISO	CCP1A	EPWM1	-
P14	-	GPIO	ANA	-	SDA0	SPI0_MOSI	CCP0A	EPWM4	-
P15	-	GPIO	ANA	-	SCL0	SPI0_SS	CCP0A	EPWM5	-
P16	-	GPIO	Note(3)	RXD0	SCL0	CTS0	CCP0B	EPWM2	ANA(3)
P17	-	GPIO	ANA	TXD0	SDA0	RTS0	CCP1A	EPWM4	-
P21	-	GPIO	ANA	RXD0	SCL0	-	CCP1B	EPWM5	BKIN
P22	-	GPIO	ANA	TXD0	SCL0	CTS1	CCP0A	EPWM0	SDA0
P23	-	GPIO	ANA	-	SDA0	RTS1	CCP0B	EPWM1	SWDDAT1(5)
P24	-	GPIO	ANA	-	SDA0	-	CCP1A	EPWM2	SWDCLK1(5)
P25	-	GPIO	ANA	-	SCL0	SPI0_SS	CCP1B	EPWM3	C1_O
P26	-	GPIO	ANA	-	-	SPI0_CLK	CCP0A	EPWM4	C0_O
P30	-	GPIO	ANA	RXD0	-	SPI0_CLK	CCP0B	EPWM0	ADET
P31	-	GPIO	ANA	CTS0	SCL0	SPI0_MISO	CCP1A	EPWM4	BKIN
P32	-	GPIO	ANA	RXD0	SDA0	SPI0_MOSI	CCP1B	EPWM1	BKIN
P34	-	GPIO	ANA	TXD0	SDA0	SPI0_CLK	CCP0A	EPWM3	BKIN
P35	-	GPIO	ANA	RTS0	SCL0	SPI0_SS	CCP0B	EPWM5	CLKO
P36	-	GPIO	ANA	-	-	CLKO	CCP1A	EPWM0	-
P40	-	GPIO	ANA	-	-	-	CCP1B	EPWM1	SWDDAT2(5)
P43	NRST	GPIO	ANA	-	-	-	CCP0A	EPWM2	-
P44	NRST	GPIO	ANA	TXD0	-	-	CCP0B	EPWM1	-
P46	-	GPIO	ANA	BKIN	-	SPI0_MISO	CCP1A	EPWM2	-
P47	-	GPIO	ANA	-	RTS1	SPI0_MOSI	CCP1B	EPWM5	-

Cont'd (TXD1 and RXD1 can be configured with any interface)

Function symbol					Function symbol			
		8	9	GPIO	ANA(multiple analog functions can be used at the same time)			
PIN	Priority	UART1	UART1	ECAP	ADC	ACMP	PGA	OP
P00	Max			-	AN0(3)	-	-	-
P01				-	AN1	-	-	-
P04				-	AN2	-	-	-
P05				-	AN3	-	-	-
P06				-	AN4	-	-	-
P07				-	AN5	-	-	-
P10				-	AN6	-	-	-
P12				-	AN7	-	A1P0	-
P13				ECAP00	AN8	C0P0	-	-
P14	↓			ECAP01	AN9	C0P1	-	-
P15				ECAP02	AN10	C0P2	A1P1	-
P16				-	AN11(3)	-	-	OP1_O(3)
P17				-	AN12	-	-	OP1_N
P21				-	AN13	-	-	OP1_P
P22				-	AN14	-	-	
P23				-	AN15	-	-	OP0_O
P24				-	AN16	-	-	OP0_N
P25				-	AN17	-	-	OP0_P
P26				-	AN18	-	-	-
P30				ECAP13	AN19	C1P3	A1P2	-
P31				ECAP10	AN20	C1P0	A0P2	-
P32	↓	TXD1	RXD1	ECAP11	AN21	C1P1	A0P1	-
P34				ECAP12	AN22	C1P2	A0O	-
P35				-	AN23	C1N	A1O	-
P36				ECAP03	AN24	C0P3	A0P0	-
P40				-	AN25	-	-	-
P43				-	AN26	C0N	A0P3	-
P44				-	AN27	-	A1P3	-
P46				-	AN28	-	-	-
P47	↓ min			-	AN29	-	-	-

Note:

(1) When configured as 0, it is GPIO and its input schmidt remains open(include when the state is output).
When configured as 1, GPIO functions, including output, schmidt input, pull-up/down are all closed.

(2) When configured as digital function, analog function is still available. For example, when configure P13 as GPIO and use ECAP function, comparator C0P0 function can also be used at the same time.

(3) When only using the analog function, it is recommended to set the configuration to 1, turn off the digital circuit to reduce power consumption. When P00 using the analog function, the configuration must be set to GPIO and input mode. The configuration of P16 must be set to 7 when using the analog function.

(4) The interface supports use at the same time of multiple analog functions, for example, P25 can use op amp function and AD channel function at the same time.

(5) SWD2(P00/P40) has debug and program function, SWD1(P23/P24) only has program function.

4. Summary of Features

4.1 ARM Cortex–M0

Cortex® -M0 is a configurable 32-bit RISC processor with multi-level pipeline. It contains a AMBA AHB-Lite interface which includes NVIC tools and has choice of configurable hardware. This processor can run Thumb instructions and it is compatible with other Cortex® -M processors. It has 2 working modes——Thread mode and Handler mod. When exception happens, system enters Handler mode and exception return is only carried out at Handler mode. After system reset or exception return, the processor can enter Thread mode.

4.2 Memory

4.2.1 Program Storage (Flash)

Program storage divided into 2 modes： APROM and BOOT. It is able to choose to boot from APROM or BOOT when power on.

Different products have different memory space. The max. space is 32KB

BOOT has max. space of 4KB.

CMS32M53xx/CMS32M55xx can configure the size of BOOT as follows:

32K(program storage)				
Address space distribution methods	APROM		BOOT	
Method 0	32K	0000H-7FFFH	-	-
Method 1	31K	0000H-7BFFH	1K	7C00H-7FFFH
Method 2	30K	0000H-77FFH	2K	7800H-7FFFH
Method 3	28K	0000H-6FFFH	4K	7000H-7FFFH

4.2.2 Non-volatile data memory (Data Flash)

It has memory of 1KB with 2 disk sectors. It is used to store and preserve the data after system shuts down.

4.2.3 Data memory (SRAM)

It has max. memory of 8KB. Every 2KB and be configured to be write-protected after the first 2KB.

4.3 Interrupt Control

Cortex®-M0 CPU provides a Nested Vector Interrupt Control (NVIC)to handle interrupts. It supports following features:

- Supports nested vector interrupt.
- Auto-save and restore the state of processor.
- Dynamic priority.
- Simplify and re-assure interrupt time.

System provides multiple external interrupt source, which include GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, CCP, WWDT, EPWM, ADC0, ADC1, ACMP, UART0, UART1, TIMER0, TIMER1, WDT, I2C, SPI and SYS_CHK. The real number of source of interrupts depends on the actual products. Each interrupt supports 4 levels of interrupt priority. The highest priority is 0 and the lowest is 3. The default priority is 0.

4.4 Clock Control

Clock controller provides the entire chip with the source of clock which includes system clock and clocks for all external devices. This controller has separated clock switch, clock source choice and frequency divider to choose different clock. It is also capable to output clock through I/O interfaces.

There are 2 different clock sources:

- Internal high-speed clock HSI (48MHz/64MHz).
- Internal low-speed clock LSI (40KHz).

Clock output can be chosen from the following:

- AHB clock AHBCLK.
- Internal high-speed clock HSI.

4.5 Power Management

4.5.1 Working Mode

The system has 4 different working modes to accommodate different power consumption needs:

- normal mode: MCU works normally, peripherals work normally, LDO enabled.
- sleep mode: MCU in sleep mode, CPU stops, peripherals work normally, LDO enabled.
- deep sleep mode: MCU in deep sleep mode, CPU stops, only WDT works, LDO enabled.
- stop mode : MCU in stop mode, CPU stop peripherals, stop LDO in low power-consuming mode.

4.5.2 Low-voltage Reset (LVR)

This series of products contains LVR. When the voltage of power source is lower than the pre-defined value, the system resets.

3 choices of low voltage detection voltage: 1.9V/2.1V/2.6V.

4.5.3 Low-voltage Detect (LVD)

This series of products contains LVD. It compares the voltage of the power source with the pre-defined value. If the power source has lower voltage, then it generates interrupt request signal.

6 choices of pre-defined values: 3.7V/3.0V/2.7V/2.4V/2.2V/2.0V.

4.6 Timer

4.6.1 System Timer (SysTick)

Cortex®-M0has a built-in system timer, SysTick. SysTick provides a simple register which is able to perform 24-bit clear on write, count down and autoloading default settings. This SysTick can be used for RTOS or peripherals for simple timer.

4.6.2 Watchdog Timer (WDT)

WDT is a 32-bit countdown timer which has a 40KHz clock source. When system enters an unknown state WDT is used to reset the system to avoid any infinite loop. WDT supports following features:

- Count clock can choose from 1, 16, 256 frequency division.
- WDT can rest system.
- WDT interrupt supported.
- WDT can resume the system from sleep /deep sleep mode.

4.6.3 Windowed Watchdog Timer (WWDT)

WWDT is a 6-bit countdown timer. WWDT is used to reset the system when entering a specific windowed period to prevent programs from running out of control. WWDT supports following features:

- Configurable 6-bit value for comparing windows.
- Count clock can choose from 14 different frequency division ratio.
- Generate interrupt when countdown value equals to the window-comparing value.
- Load data and generate system reset when countdown value is greater than window-comparing value.
- Reset system when countdown to 0

4.6.4 General Timer (TIMER0/1)

This series of products contains 2 programmable 32/16-bit counter(countdown) to provide user with convenient counting application. TIMER0 and TIMER1 supports following features:

- Count clock can choose from 1, 16, 256 frequency division.
- 3 operating modes: single-triggered, periodic counting, continuous counting.
- Support delay loading of initial value of counter
- Generate interrupt when countdown to 0
- Resume sleep mode from interrupt.

4.7 Enhanced Digital Peripherals

4.7.1 Cyclic Redundancy Check (CRC)

CRC is a commonly used error-detecting code. The main feature is that any choice of length of information data and verification data is possible. CRC verification unit generates polynomial '$X^{16}+X^{12}+X^5+1$'(CRC-16-CCITT). The data that needs to be checked is selected from programs, therefore this module is not only used in program flash space but many other places.

4.7.2 Hardware Divider (HWDIV)

This series of products contains a 32bit/32bit hardware divider with the following features:

- Support division of sign/unsigned number.
- Contains indicator when divide 0.
- Quotient and remainder have 32-bit bit width.
- Write on divisor register to start division calculation.
- 6 HCLK clock for calculation

4.7.3 Capture/Compare/Pulse Width Modulation Modules (CCP0/1)

This series of products contains 2 sets of CCP modules: CCP0/CCP1. Each CCP corresponds to A/B channels. CCP modules support PWM output, capture mode 0, capture mode 1, interrupt.

1) PWM output supports following features:

- A, B channels of CCP0 share a periodic register. A, B channels of CCP1 share a periodic register.
- Can configure duty cycle of A, B channels' output separately.
- Max. 4 output of PWM.
- Configurable output polarity.

2) capture mode 0 supports following features:

- CCP0 can choose from A or B as external input signal.
- CCP1 can choose from A or B as external input signal.
- 4 methods of capture:
  a) software initiated counting, rising edge capture;
  b) software initiated capture, falling edge capture;
  c) rising edge counting, falling edge capture;
  d) falling edge capture, rising edge capture.

3) capture mode 1 supports following features:

- Only CCP1 has capture mode 1.
- CAP0, CAP1, CAP2, CAP3, altogether 4 capture channels, each capture channel has 4 bits to choose different inputs.
- Can choose register triggered software capture mode.
- Can choose rising edge, falling edge and double edge of external signal for capture mode.
- Support CCP1 capture trigger CCP0 counter load enabled.

4) CCP has following interrupts:

- PWM interrupt.
- Capture mode 0 interrupt.
- CAP0, CAP1, CAP2, CAP3 interrupts in capture mode 1.
- Counter overflow interrupt.

4.7.4 Enhanced PWM (EPWM)

Enhanced PWM module has 6 PWM generators. Period and duty cycle can be configured separately. EPWM supports following features:

- Support single/continuous output of waveform.
- Support 4 control modes: individual/complementary/synchronous/grouped.
- Counter clock choices: 1, 2, 4, 8, 16 frequency division.
- Support 2 counting modes: edge-aligned/center-aligned.
- Support 4 methods of load updates.
- Support dead-time insertion.
- Configurable output polarity.
- Support periodic, up-comparison, down-comparison and zero interrupt.

4.8 Communication Modules

4.8.1 Universal Asynchronous Receiver-Transmitter (UART0/1)

This series of products contain 2 interfaces: UART0 and UART1.UART has following characteristics：

- Full duplex, asynchronous communication.
- Register structure satisfy 16550 industrial standards.
- Separated 16 byte transmit/receive FIFO.
- Support hardware auto flow control (CTS, RTS.).
- Support software flow control (XOFF, XON).
- Choice of level of receive data buffer.
- Data length can be set to 5-8.
- Stop bit can be set to 1-bit, 1.5-bit or 2-bit.
- Check bit can be set to odd/even/none/fixed.

4.8.2 I²C Inter-Integrated Circuit (I²C)

This series of products contains a 2-wire serial control, I2C. It supports following features:

- Standard I2C compatible of bus interface.
- Support master /slave mode. Bidirectional data transfer between master and slave.
- Arbitration during multi master data transfer to avoid serial data damage on the bus.
- Bus with serial synchronous clock to achieve different transfer speed between different devices.
- Programmable clock for transfer speed control.
- Support 7/ 10bit address mode.
- Support multi address identification.

4.8.3 Serial Peripheral Interface (SSP/SPI)

This series of products contains 1 full duplex and synchronous SSP/SPI. SSP/SPI supports following features：

- Compatible of: SPI from Motorola, 4 wire SSI from TI and Microwire bus from NS.
- Support master or slave mode.
- Configurable length of send bit.
- Configurable clock polarity and phase.
- Programmable clock speed control.
- Provides eight 16-bit transmit/receive FIFO.

4.9 Analog Module

4.9.1 Low Speed ADC (ADC0)

This series of products contains a 12-bit successive approximation ADC (ADC0) which supports single/continuous converting modes. ADC0 supports the following features:

- Analog input voltage range: AVSS(VSS) ~ AVDD(VDD).
- Max. sampling rate: 100Ksps.
- 24 single-ended analog input channels.
- Single conversion time of 18.5*T_{ADCK}.
- Single mode: carry a A/D convert to a selected channel.
- Continuous mode: carry A/D convert for all selected channels.
- Support external input signal to trigger ADC.
- Generate interrupt after finishing converting.
- Built-in ADC result comparator.
- ADC results from every channel are stored to respective data registers.
- Channel 30 can test internal analog voltage signal (including OP0/1output, PGA0/1output, built in 1.2V reference voltage)

4.9.2 Fast ADC (ADC1)

This series of products contains a 12-bit successive approximation ADC (ADC1) which supports single/continuous converting modes. The fastest conversion time for single mode ADC is about 0.8us. The fastest total conversion time for continuity mode of any of the 4 channel ADC is about 3.2us, 12.8us for 16 channel ADC. ADC1 supports following features:

- Analog input voltage range: AVSS(VSS) ~ AVDD(VDD).
- Max. sampling rate: 1.2Msps.
- 24 single-ended analog input channels.
- Single conversion time of: 23*T_{ADCK} (sampling time set to 10.5*T_{ADCK}).
- Single mode: carry a A/D convert to a selected channel.
- Continuous mode: carry A/D convert for all selected channels.
- Support external input signal to trigger ADC
- Generate interrupt after finishing converting.
- Built-in ADC result comparator.
- ADC results from every channel are stored to respective data registers.
- Channel 30 can test internal analog voltage signal (including OP0/1output, PGA0/1output, built in 1.2V reference voltage)

4.9.3 Analog Comparator (ACMP0/1)

This series of products contains 2 analog comparators,ACMP0 and ACMP1. ACMP0/1 supports following features:

- Analog input voltage range: 0~(VDD-1.5V).
- Support hysteresis voltage choice (10mV/20mV/60mV-typical value).
- Positive end can choose multiple input interfaces.
- Negative end can choose input interface or internal reference voltage.
- 16 levels of internal reference voltage division.
- Support output filter with 11 choices of filters.
- Support change in output to generate interrupt.

4.9.4 Operational Amplifier (OP0/1)

This series of product contains OP0 and OP1 which supports following features:

- Can configure to operational amplifier mode or comparator mode.
- Adjustable offset voltage.
- Measure output through ADC.

4.9.5 Programmable Gain Amplifier (PGA0/1)

This series of products contains 2 programmable gain amplifier PGA0 and PGA1 which supports the following features

- Adjustable gain(4X/8X/10X/12X/14X/16X/32X).
- Measure output through ADC.

4.10 Memory Control Module

FLASH memory includes program memory (APROM/BOOT) and non-volatile data memory (Data FLASH). It is possible to read/write through relative special function (SFR) registers to achieve IAP function. FLASH memory supports the following:

- Byte reading
- Byte writing
- Page erase
- FLASH CRC.

4.11 Security

4.11.1 Unique Identifier (UID)

Every chip has 96-bit UID which is set during manufacture. Users can only read but not modify.

4.11.2 User Unique Identifier (USRUID)

Every chip has a 128-bit USRID, which includes 96-bit user-configurable ID and a 32-bit fixed ID. This USRUID cannot be accessed from memory module. USRUID can be used as key in during encryption of some applications. Users can set protection through checking this key.

4.11.3 Protection of Code for Programs

Support protection of codes through partition and distribution. In APROM space, every 2Kbytes is a chunk. In BOOT space, every 1Kbytes is a chunk. Users can configure protection state from config registers.

4.11.4 Program CRC

Support hardware to calculate CRC verification code. Choice of check interval is allowed. CRC verification code is generated from polynomial CRC-16-CCITT '$X^{16}+X^{12}+X^5+1$'.

4.11.5 General CRC

Use general CRC to check the correctness of program or transferred data. Verification code for general CRC module is also generated from polynomial '$X^{16}+X^{12}+X^5+1$'.

4.11.6 Unauthorized Read/Write Detection of Memory

If authorized memory address in ARM MCU is accessed, bus will return an error signal to provide better program error detection.

4.11.7 SRAM Protection

Internal SRAM is write-protected and can be configured to distributed storage. Write-protection does not affect reading process. Relative functions can be set from system register SRAMLOCK.

4.11.8 SFR Protection

SFR in key modules has protection state. Reading/writing is disabled under the protection state.

4.11.9 ADC0/1 Test

Check whether ADC is working properly through converting ADC's positive reference voltage, negative reference voltage, analog input channel, internal reference voltage.

4.11.10 GPIO Pin Electrical Level Detection

It is possible to read pin's electrical level through GPIO->DI when interface is configured as output or input under GPIO.

5. User Configuration

User configuration area is a 128-word (512 bytes) storage area allocated in FLASH. Following features can be achieved through setting the registers:

- LVR reset voltage
- Power-On reset bootup space (APROM/BOOT) .
- User programs, User UID, Data-Flash encryption control.
- Power-On WDT enable control, initial loading value.
- SWD debug function.
- External reset function and pin distribution.

6. Electrical Characteristics

6.1 MCU Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}-V_{SS}	voltage	-0.3	5.8	V
V_{IN}	Input voltage	VSS-0.3	VDD+0.3	V
T_A	Operating temperature	-40	+105	℃
T_{ST}	storage temperature	-55	+150	℃
I_{DD}	VDD maximum input current	-	120	mA
I_{SS}	VSS maximum output current	-	120	mA
I_{IO}	Single IO maximum sink current	-	50	mA
	Single IO maximum output current	-	40	mA
	All IO maximum sink current	-	100	mA
	All IO maximum output current	-	100	mA

6.2 D.C Electrical Characteristics

(V_{DD}-V_{SS}=2.1~5.5V,T_A=25℃)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Voltage	HCLK=64MHz	2.1	-	5.5	V
I_{DD1}	operating current	HCLK=64MHz, HSI=64MHz, ALL APBCLK OFF, V_{DD}=5.0V	-	12	-	mA
I_{DD2}		HCLK=64MHz, HSI=64MHz, ALL APBCLK OFF, V_{DD}=3.3V	-	12	-	mA
I_{DD3}		HCLK=48MHz, HSI=48MHz, ALL APBCLK OFF, V_{DD}=5.0V	-	9	-	mA
I_{DD4}		HCLK=48MHz, HSI=48MHz, ALL APBCLK OFF, V_{DD}=3.3V	-	9	-	mA
I_{DD5}		HCLK=40KHz, LSI=40KHz, ALL APBCLK OFF, V_{DD}=5V	-	0.25	-	mA
I_{DD6}		HCLK=40KHz, LSI=40KHz, ALL APBCLK OFF, V_{DD}=3.3V	-	0.25	-	mA
I_{DEEP_SLEEP}	Deep sleep mode current	LDO on, V_{DD}=5V	-	200	-	uA
I_{SLEEP}	Stop mode current	LDO in low power mode, V_{DD}=5V	-	10	-	uA
V_{IL}	Input low level	-	VSS	-	0.3VDD	V
V_{IH}	Input high level	-	0.7VDD	-	VDD	V
I_{OL1}	Low-level output current	V_{DD}=5V GPIOxDR[n]=0 VIO=1.5V	-	-	50	mA
I_{OL2}		V_{DD}=5V GPIOxDR[n]=1 VIO=1.5V	-	-	25	mA
I_{OH1}	High-level output current	V_{DD}=5V GPIOxDR[n]=0 VIO=3.5V	-	-	40	mA
I_{OH2}		V_{DD}=5V GPIOxDR[n]=1 VIO=3.5V	-	-	20	mA
R_{UP}	Pull-up resistor	-	-	33	-	KΩ
R_D	Pull-down resistor	T_A=25℃, VDD=5V, V_{IO}=0.3VDD	-	33	-	KΩ
F_{AHBCLK}	AHB clock	-	-	-	64	MHz
F_{APBCLK}	APB clock	-	-	-	64	MHz

6.3 MCU A.C. Electrical Characteristic

6.3.1 Power-on Reset Time

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{RESET}	Reset time	VDD=5V	-	4.5	-	ms
T_{VDDR}	VDD rise rate	VDD=5V	2	-	-	us/V
T_{VDDF}	VDD fall rate	VDD=5V	2	-	-	us/V

6.3.2 Internal High-speed Oscillator (HSI)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{HSI}	Operating voltage	2.1	-	5.5	V
T_A	Operating temperature	-40	-	105	℃
I_{HSI}	operating current V_{DD}=5.0V,T_A=25℃	-	300	-	uA
F_{HSI48M}	T_A=25℃,V_{DD}=5.0V	-	48	-	MHz
	T_A=25℃,V_{DD}=2.1~5.5V	-0.5	-	+0.5	%
	T_A=0℃~85℃,V_{DD}=2.1~5.5V	-1.5	-	+1.0	%
	T_A=-40℃~105℃,V_{DD}=2.1~5.5V	-2.0	-	+1.0	%
F_{HSI64M}	T_A=25℃,V_{DD}=5.0V	-	64	-	MHz
	T_A=25℃,V_{DD}=2.1~5.5V	-0.5	-	+0.5	%
	T_A=0℃~85℃,V_{DD}=2.1~5.5V	-2.0	-	+1.0	%
	T_A=-40℃~105℃,V_{DD}=2.1~5.5V	-2.5	-	+1.0	%

6.3.3 Internal low-speed Oscillator (LSI)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LSI}	Operating voltage	2.1	-	5.5	V
T_A	Operating temperature	-40	-	105	℃
I_{LSI}	operating current V_{DD}=5.0V,T_A=25℃	-	10	-	uA
F_{LSI}	T_A=25℃,V_{DD}=5.0V	-	40	-	KHz
	T_A=25℃,V_{DD}=2.1~5.5V	-5.0	-	+5.0	%
	T_A=-40℃~105℃,V_{DD}=2.1~5.5V	-50	-	+50	%

6.3.4 Low Voltage Reset Electrical Parameters (LVR)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LVR1}	Low-voltage detection threshold 1.9V	1.75	1.9	2.05	V
V_{LVR2}	Low-voltage detection threshold 2.1V	1.95	2.1	2.25	V
V_{LVR3}	Low-voltage detection threshold 2.6V	2.45	2.6	2.75	V

6.3.5 Low Voltage Detection Circuit (LVD)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{LVD1}	Low-voltage detection threshold 2.0V	1.85	2.0	2.15	V
V_{LVD2}	Low-voltage detection threshold 2.2V	2.05	2.2	2.35	V
V_{LVD3}	Low-voltage detection threshold 2.4V	2.25	2.4	2.55	V
V_{LVD4}	Low-voltage detection threshold 2.7V	2.55	2.7	2.85	V
V_{LVD5}	Low-voltage detection threshold 3.0V	2.85	3.0	3.15	V
V_{LVD6}	Low-voltage detection threshold 3.7V	3.55	3.7	3.85	V

6.4 FLASH Electrical Parameters

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_F	Flash operating voltage	-	2.1	-	5.5	V
T_F	Flash operating temperature	-	-40	25	125	℃
$N_{ENDURANCE}$	Endurance	-	20,000	-	-	Cycle
T_{RET}	Data Retention	25℃	100	-	-	year
T_{ERASE}	Sector Erase Time	-	-	4.7	-	ms
T_{PROG}	Program Time	-	-	7	-	us
I_{DD1}	Read Current	-	-	-	3.5	mA
I_{DD2}	Program Current	-	-	-	3.5	mA
I_{DD3}	Erase Current	-	-	-	2	mA

6.5 Analog Electrical Characteristics

6.5.1 BANDGAP Electrical Characteristic

VDD=2.1V-5.5V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REF}	Internal reference 1.2V	T_A=-40℃ ~ 105℃	1.188	1.2	1.212	V

6.5.2 ADC0 Electrical Characteristic

TA = 25℃.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{AVDD}	ADC operating voltage	2.5	-	5.5	V
V_{REF}	Reference voltage	-	V_{AVDD}	-	V
V_{ADI}	Analog signal input	0	-	V_{REF}	V
N_R	Resolution	12			Bit
DNL	Differential non-linearity error (V_{REF}=V_{AVDD}=5V,T_{ADCK}=0.5us)	±4			LSB
INL	Integral non-linearity error (V_{REF}=V_{AVDD}=5V,T_{ADCK}=0.5us)	±5			LSB
T_{ADCK}	ADC clock cycle	0.5	-	32	us
T_{ADC}	ADC conversion time	-	18.5	-	T_{ADCK}
F_S	Sampling rate (V_{REF}=V_{AVDD}=5V)	100			Ksps

6.5.3 ADC1 Electrical Characteristic

TA = 25℃.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{AVDD}	ADC operating voltage	2.5	-	5.5	V
V_{REF}	Reference voltage	-	V_{AVDD}	-	V
V_{ADI}	Analog signal input	0	-	V_{REF}	V
N_R	Resolution	12			Bit
DNL	Differential non-linearity error (T_{ADCK}=0.0625us, T_{ADC}=23 *T_{ADCK})	±4			LSB
INL	Integral non-linearity error (T_{ADCK}=0.0625us, T_{ADC}=23 *T_{ADCK})	±5			LSB
T_{ADCK}	ADC clock cycle	0.0325	-	5.3	us
T_{ADC}	AD conversion time (Sample hold time:10.5*T_{ADC})	-	23	-	T_{ADCK}
F_C	Conversion rate	1.4			Msps
F_S	Sampling rate	1.2			Msps

6.5.4 OP0/1 Electrical Parameter

T_A = 25℃,V_{SENSE} = V_{IN+} -V_{IN-},VDD = 5V,V_{IN+}=1V,Unless otherwise indicated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	-	2.5	-	5.5	V
I_Q	Quiescent Current	V_{SENSE}=0mV	-	0.8	1.3	mA
I_{SD}	Shutdown current	-	-	5	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input Characteristic						
V_{OS}	Input Offset Voltage	No zero adjustment	-	±3.8	-	mV
		After zero adjustment	-	±0.5	-	
V_{CM}	Common-mode Input Range	-40℃~105℃	0	-	VDD-1.5	V
I_B	Input Bias Current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset Current	V_{SENSE}=0mV	-	10	-	pA
Output Characteristic						
C_{LOAD}	Capacitive load	-	-	30	-	pF
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD-0.3	V
V_{OL}	Minimum output voltage	-40℃~105℃	0.3	-	-	V
Frequency characteristic						
A_{OL}	Open loop gain	-	-	105	-	dB
BW	Bandwidth	C_{LOAD}=30pF	-	5	-	MHz
PSRR	Power Supply Rejection Ratio	VDD=2.5~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	59	-	dB
CMRR	Common Mode Rejection Ratio	V_{IN+}=0.3~(VDD-1.5) -40℃~105℃	-	110	-	dB
Transient characteristic						
SR	Slew Rate	C_{LOAD} =30pF	-	±5	-	V/μs
		R_{LOAD}=2K,C_{LOAD}=100pF	-	±4	-	V/μs
T_{STB}	Stable Time	-	-	-	1.5	μs

6.5.5 ACMP0/1 Electrical Parameter

T_A = 25℃, V_{SENSE} = V_{IN+}-V_{IN-}, VDD = 5V, V_{IN+}=1V, Unless otherwise indicated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	-	2.1	-	5.5	V
I_Q	Quiescent Current	V_{SENSE}=0.1V	-	0.3	0.4	mA
I_{SD}	Shutdown current	V_{SENSE}=0.1V	-	5	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input Characteristic						
V_{OS}	Input Offset Voltage	No zero adjustment	-	±4.0	-	mV
		After zero adjustment	-	±0.5	-	
V_{CM}	Common-mode Input Range	-40℃~105℃	-0.1	-	VDD-1.5	V
I_B	Input Bias Current	V_{SENSE}=0mV	-	10	-	pA
I_{OS}	Input offset Current	V_{SENSE}=0mV	-	10	-	pA
V_{HYS}	Input hysteresis voltage	VDD=2.1~5.5V, V_{IN+}=0.5V	-	0 ±10 ±20 ±60	-	mV
Output Characteristic						
V_{OH}	Maximum output voltage	-40℃~105℃	-	-	VDD	V
V_{OL}	Minimum output voltage	-40℃~105℃	0	-	-	V
Frequency characteristic						
A_{OL}	Open loop gain	-	-	85	-	dB
BW	Bandwidth	-	-	120	-	MHz
PSRR	Power Supply Rejection Ratio	VDD=2.1~5.5V, V_{IN+}=1V, V_{SENSE}=0mV	-	80	-	dB
CMRR	Common Mode Rejection Ratio	VDD=2.1~5.5V, -40℃~105℃	-	90	-	dB
Transient characteristic						
T_{STB}	Stable Time	-	-	-	1.5	μs
T_{PGD}	Response dela	V_{COM}=1V, V_{IN+}= V_{IN-} ±0.1V	-	50	100	ns

6.5.6 PGA0/1 Electrical Parameter

T_A = 25℃, VDD = 5V, V_{IN+}=0.1V, Unless otherwise indicated.(G is the gain multiple).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	-	2.5	-	5.5	V
I_Q	Quiescent Current	V_{OUT}=2V	-	0.9	1.6	mA
I_{SD}	Shutdown current	-	-	10	-	nA
T_A	Operating temperature	-	-40	25	105	℃
Input Characteristic						
V_{OS}	Input Offset Voltage	-	-	±3.0	-	mV
V_{CM}	Common-mode Input Range	-40℃~105℃	0.07*VDD/ G	-	0.93*VDD/ G	V
I_B	Input Bias Current	-	-	10	-	pA
I_{OS}	Input offset Current	-	-	10	-	pA
Output Characteristic						
EG	Gain error	G=4,8	-1	-	1	%
		G=10,12,14,16	-1.5	-	1.5	
		G=32	-2	-	2	
C_{LOAD}	Capacitive load	-	-	10	-	pF
V_{OH}	Maximum output voltage (internal)	-40℃~105℃	-	VDD-0.3	-	V
V_{OL}	Minimum output voltage	-40℃~105℃	-	0.3	-	V
V_{A0O} V_{A1O}	Test output interface of PGA0/1 (A0O, A1O)	-40℃~105℃	-	-	3.7	V
Frequency characteristic						
BW	Bandwidth	R_{LOAD}=0.8MΩ, C_{LOAD}=3pF, G=4	-	2	-	MHz
PSRR	Power Supply Rejection Ratio	VDD=2.5~5.5V	-	75	-	dB
CMRR	Common Mode Rejection Ratio	-40℃~105℃	-	80	-	dB
Transient characteristic						
SR	Slew Rate	R_{LOAD}=0.8MΩ, C_{LOAD}=3pF	-	6	-	V/μs
		R_{LOAD}=2KΩ, C_{LOAD}=100pF	-	4	-	V/μs
T_{STB}	Stable Time	-	-	-	2	μs

6.6 GATE DRIVER(6N) Electrical Characteristic (CMS32M5533)

6.6.1 Static Electrical Characteristic Parameters

(VCC-COM) =(VB-VS)=15V. Without other explanation,otherwise the reference temperature is TA=25 ℃ .Input parameters of all channels VIN, TH, VI, and IIN on COM pin for reference. Likewise, Output parameters of all low edge driver VO and IO on COM pin for reference. However, output parameters of all high edge driver VO and IO with their own VS for reference. VCCUV parameter on COM for reference. VBSUV parameter on VS for reference.

Symbol	Parameter	Condition	Min	Typical	Max	Unit
Low edge characteristics of power supply						
I_{QVCC1}	Static VCC power supply current	$V_{HIN1,2,3}$ =$V_{LIN1,2,3}$=0 or 5V, V_{ENB}=0	210	330	450	μA
I_{QVCC2}	Static VCC power supply current in standby mode	$V_{HIN1,2,3}$ =$V_{LIN1,2,3}$=0 or 5V, V_{ENB}=5	-	46	80	
I_{VCCOP}	Dynamic VCC power supply current	$f_{LIN1,2,3}$=20KHz, $f_{HIN1,2,3}$=20KHz,	-	1500	-	
V_{CCUV+}	VCC power supply under voltage lock positive threshold voltage	-	2.9	4.2	5.5	V
V_{CCUV-}	VCC power supply under voltage lock negative threshold voltage	-	2.5	3.8	5.1	
V_{CCHYS}	VCC power supply under voltage lock magnetic hysteresis voltage	-	-	0.4	-	
High edge floating characteristics of power supply						
V_{BSUV+}	High edge VBS power supply under voltage lock positive threshold voltage	-	2.5	3.8	5.5	V
V_{BSUV-}	High edge VBS power supply under voltage lock negative threshold voltage	-	2.2	3.5	4.8	
$V_{BSUVHYS}$	High edge VBS power supply under voltage lock magnetic hysteresis voltage	-	-	0.3	-	
I_{QBS}	High edge static VBS power supply current	V_{BS}=15V	25	45	65	μA
I_{LK}	High edge leakage current	V_B=V_S=100V V_{CC}=0V	-	-	10	
Logic input characteristic						
V_{IH}	HIN1,2,3, LIN1,2,3 and ENB=logic “1” voltage	-	2.5	-	-	V
V_{IL}	HIN1,2,3, LIN1,2,3 and ENB logic “0” voltage	-	-	-	0.8	
$V_{IN,\ TH+}$	Input positive threshold voltage	-	-	1.9	-	
$V_{IN,\ TH-}$	Input negative threshold voltage	-	-	1.4	-	
I_{IN+}	Logic “1” input bias current	V_{IN}=5V	-	50	-	μA
I_{IN-}	Logic “0” input bias current	V_{IN}=0	-	0	-	
Characteristics of gate driver						
I_{HO+}	High edge driver output “high” short-circuited current (withdraw)	V_{HO}=V_S=0	-	1.2	-	
I_{HO-}	High edge driver output “low” short-circuited current (entrance)	V_{HO}=V_B=15V	-	2.0	-	
I_{LO+}	Low edge driver output “high” short-circuited current (withdraw)	V_{LO}=0	-	1.2	-	
I_{LO-}	Low edge driver output “low” short-circuited current (entrance)	V_{LO}=V_{CC}=15V	-	2.0	-	
V_{SN}	Negative VS voltage can be allowed when HIN signal is normally transmitted to HO	V_{BS}=15V	-	-8	-	V

6.6.2 Dynamic Electrical Characteristic Parameters

Without other explanation, otherwise all are (VCC-COM) =(VB-VS)=15V ,$V_{S1,2,3}$=COM, and C_{load}=1nF, the temperature of surrounding environment T_A=25℃.

Symbol	Parameter	condition	Min	Typical	Max	Unit
T_{on}	Turn-on transmission delay	VHIN1,2,3 or $V_{LIN1,2,3}$=5V, $V_{S1,2,3}$=0	-	120	200	ns
t_{off}	Turn-off transmission delay	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=0, $V_{S1,2,3}$=0	-	120	200	
t_r	Turn-on rise time	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=5V, $V_{S1,2,3}$=0	-	37	-	
t_f	Turn-off fall time	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=0, $V_{S1,2,3}$=0	-	30	-	
DT	Dead time	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=0~ 5V, No external dead time	300	500	700	
MDT	Six channels dead time match	No external dead time	-	-	50	
MT	Six channels delay match	external dead time > 1000ns	-	-	50	
PM	Output pulse width match	external dead time > 1000ns, PW_{IN}=10μs, $PM=PW_{OUT}–PW_{IN}$	-	-	50	
$t_{FLT, ENB}$	ENB input filtering time width	V_{ENB}=0 ~ 5V	-	450	-	
$t_{off, ENB}$	ENB input “high” to HO/LO turn-off delay	V_{ENB}=5V	-	0.55	-	μs
$t_{on, ENB}$	ENB input “low” to HO/LO turn-on delay	V_{ENB}=0V	-	6	-	

6.7 GATE DRIVER(6N) Electrical Characteristic (CMS32M5536)

6.7.1 Absolute Maximum Ratings

(Unless otherwise indicated, T_A=25℃, GND as a reference point for all pins).

Parameter	Symbol	Min	Max	Unit
High side floating offset absolute voltage	$VB_{1,2,3}$	-0.3	225	V
High side floating offset relative voltage	$VS_{1,2,3}$	$VB_{1,2,3}$-25	$VB_{1,2,3}$+0.3	V
High side output voltage	$V_{HO1,2,3}$	$VS_{1,2,3}$-0.3	$VB_{1,2,3}$+0.3	V
Maximum power supply	VCC	-0.3	25	V
Low side output voltage	$V_{LO1,2,3}$	-0.3	VCC	V
Maximum power supply (HIN1,2,3/LIN1,2,3)	V_{IN}	-0.3	10	V
Maximum voltage slew rate of offset voltage	dVS/dt	-	50	V/ns
Maximum power consumption (note 1)	P_D	-	1.25	W
Environmental thermal resistance	θ_{JA}	-	100	℃/W
Junction temperature	T_J	-	150	℃
Storage temperature	T_s	-55	150	℃
Welding temperature of pins (duration 10s)	T_L	-	260	℃
ESD (note 2)	V_{ESD}	-	2000	V

Note:

1) In any case, don't over P_D, the calculation formula of maximum power dissipation under different environmental tempera: $P_D=(150℃-T_A)/\theta_{JA}$
   T_A is the environmental temperature, θ_{JA} is package thermal resistance, the highest junction temperature for the circuit is 150℃;
2) Human model, 100pF capacitor is discharged through the 1.5KΩ resistor;
3) When the working conditions of circuit exceed the range specified by the absolute maximum ratings, it is likely to cause immediate damage to the circuit.

6.7.2 Recommended working conditions

(Unless otherwise indicated, T_A=25℃, GND as a reference point for all pins).

Parameter	Symbol	Min	Typical	Max	Unit
High side floating offset absolute voltage	$VB_{1,2,3}$	$VS_{1,2,3}$+8	$VS_{1,2,3}$+15	$VS_{1,2,3}$+20	V
High side floating offset relative voltage	$VS_{1,2,3}$	GND-5	-	200	V
High side output voltage	$V_{HO1,2,3}$	$VS_{1,2,3}$	$VS_{1,2,3}$+15	$VB_{1,2,3}$	V
Power supply	V_{CC}	8	15	20	V
Low side output voltage	$V_{LO1,2,3}$	0	15	V_{CC}	V
Input voltage (HIN1,2,3 /LIN1,2,3)	V_{IN}	0	-	5	V
Range of working temperature (note 1)	T_{opr}	-20	-	+85	℃

Note:

1) T_{opr} means the environmental temperature of the circuit;

2) Working outside the recommended conditions for a long time may affect its reliability, it is not recommended that the chip work beyond the recommended working conditions for a long time.

6.7.3 Electrical Characteristic parameter table

(TA=25℃, VCC=$VBS_{1,2,3}$=15V, $VS_{1,2,3}$=GND, GND as a reference point for all pins, Unless otherwise indicated)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Power supply current parameters						
VCC static current	I_{CCQ}	V_{IN}=0V	200	300	450	uA
VBS static current	I_{BSQ}	V_{HIN}=0V	30	48	70	uA
VCC dynamic current	I_{CCD}	$f_{LIN1,2,3}$=20kHz	-	560	-	uA
VBS dynamic current	I_{BSD}	$f_{HIN1,2,3}$=20kHz	-	180	-	uA
VB floating power supply leakage current	I_{LK}	VB=225V	-	-	0.1	uA
Power supply voltage parameters						
VCC undervoltage high-level potential	VCC_{HY+}		6.5	7	7.5	V
VCC undervoltage high-level potential	VCC_{HY-}		5.8	6.3	6.8	V
VCC undervoltage hysteresis level	VCC_{HY}		0.4	0.7	-	V
VBS undervoltage high-level potential	VBS_{HY+}		6.5	7	7.5	V
VBS undervoltage high-level potential	VBS_{HY-}		5.8	6.3	6.8	V
VBS undervoltage hysteresis level	VBS_{HY}		0.4	0.7	-	V
VS static negative voltage	VS_{QN}		-	-5.0	-	V
Input parameters						
Input high level current	I_{IN+}	V_{IN}=5V	-	50	70	uA
Input low level current	I_{IN-}	V_{IN}=0V	-	0	1	uA
Input high level potential	V_{IN+}		2.6	-	-	V
Input low level potential	V_{IN-}		-	-	0.8	V
Input hysteresis level	V_{INHY}		-	1.2	-	V
Output parameters						
High level shot-circuit pulse current	I_{OUT+}	V_{IN}=5V V_O=0V PWD≤10μs	0.8	1.1	1.4	A
Low level short-circuit pulse current	I_{OUT-}	V_{IN}=0V V_O=15V PWD≤10μs	1.5	2.0	2.5	A
High level output voltage	V_{OUT+}	I_{OUT}=-100mA	14.20	14.48	-	V
Low level output voltage	V_{OUT-}	I_{OUT}=+100mA	-	0.17	0.35	V
Time parameters						
Output rising edge transmission time	t_{ON}	No Load	-	220	-	ns
Output falling edge transmission time	t_{OFF}	No Load	-	220	-	ns
Output rising time	t_r	C_L=3.3nF	-	50	80	ns
Output falling time	t_f	C_L=3.3nF	-	23	40	ns
Dead time	DT	No Load	-	310	-	ns
High and low side match time	MT		-	-	50	ns

6.8 GATE DRIVER(3P3N) Electrical Characteristic (CMS32M5524)

6.8.1 Absolute Maximum Ratings

CMS32M5512 (Unless otherwise indicated, TA=25℃)

Parameter	Symbol	Range			Unit
		Min	Typical	max	
Power supply voltage	GVDD	8	12	16	V
Input frequency	Fin	-	-	100	KHz

CMS32M5524 (Unless otherwise indicated, T_A=25℃) .

Parameter	Symbol	Range			Unit
		Min	Typical	Max	
Power supply voltage	GVDD	16	24	30	V
Input frequency	Fin	-	-	100	KHz

6.8.2 Electrical characteristic parameters

6.8.2.1 Driving NMOS power transistors

(Unless otherwise indicated, VDD=12V, T_A=25℃) .

Parameter	Symbol	Range			Unit
		Min	Typical	max	
Power supply voltage	GVDD	8	12	16	V
Input frequency	Fin	-	-	100	KHz

6.8.2.2 Driving PMOS power transistors

(Unless otherwise indicated, VDD=12V, T_A=25℃) .

Parameter	Condition	Min	Typical	Max	Unit
I_{in}P*_IN input current	V_{P*_IN}=5V	0.7	0.9	1.1	mA
V_{OH} output high level	NO Load	10.5	11	-	V
V_{OL} output low level	NO Load	-	-	1	
tPHH rise edge delay	VDD=12V, NO Load	-	75	150	ns
tPLL fall edge delay		-	75	150	
tr rise edge	VDD=12V, CL=1nF	-	100	300	
tf fall edge	VDD=12V, CL=1nF	-	100	300	

6.8.3 Time Parameter Test Description

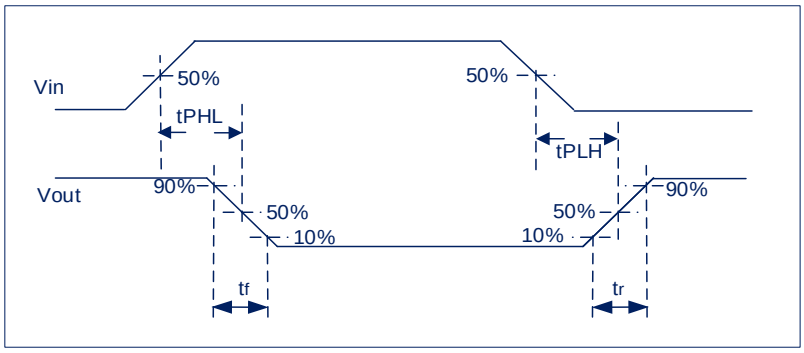
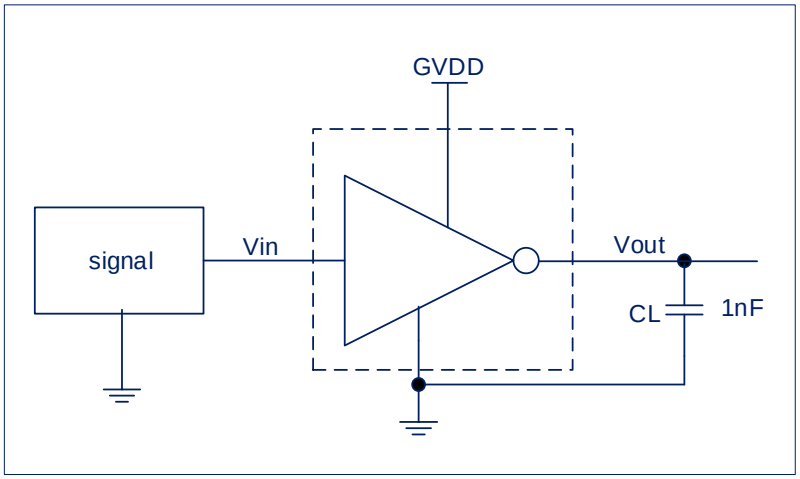
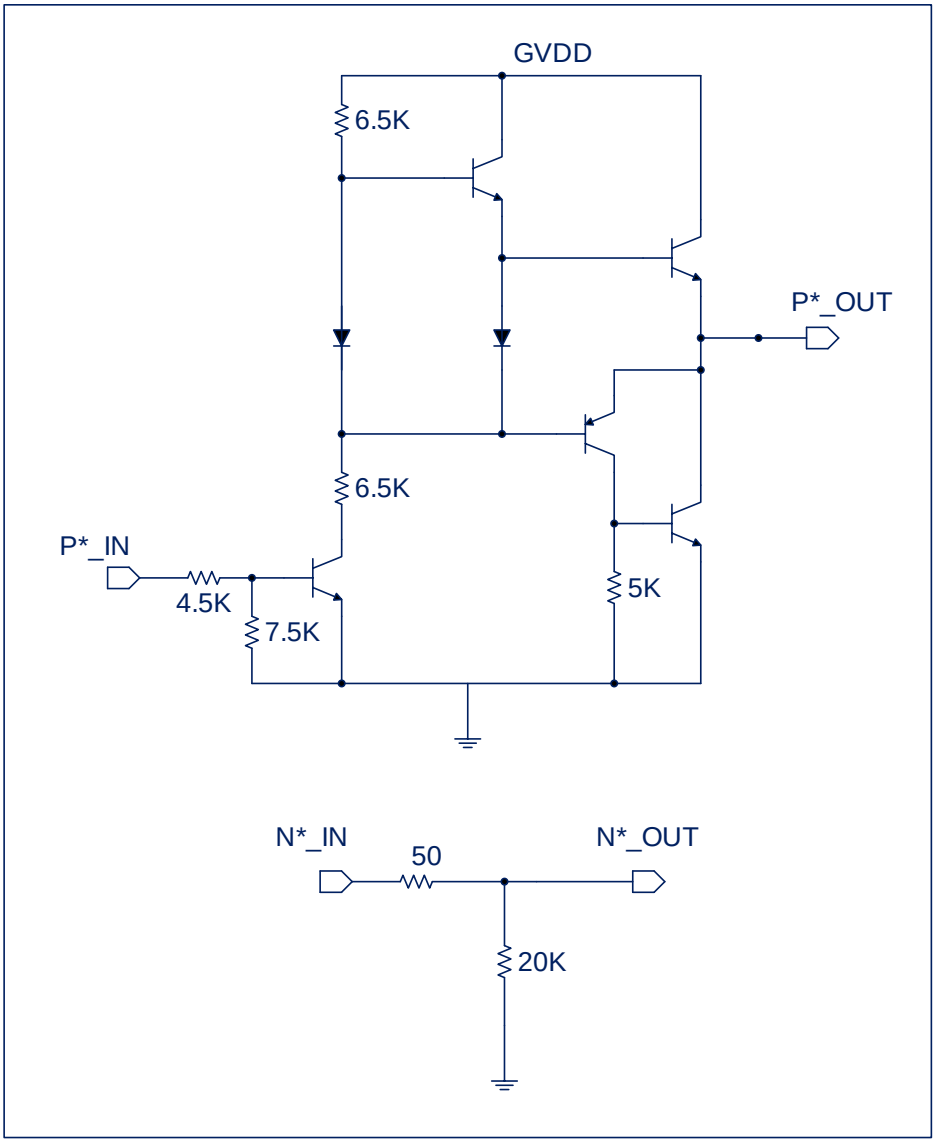


Diagram of time parameter test



Block diagram of test circuit

6.8.4 3P3N Pre-driver Internal Logic Block Diagram Characteristic



3P3N pre-driver internal logic block diagram

6.8.5 Logical Truth Table

NMOS Logical Truth Table

N*_IN	N*_OUT
Hanging	L
L	L
H	H

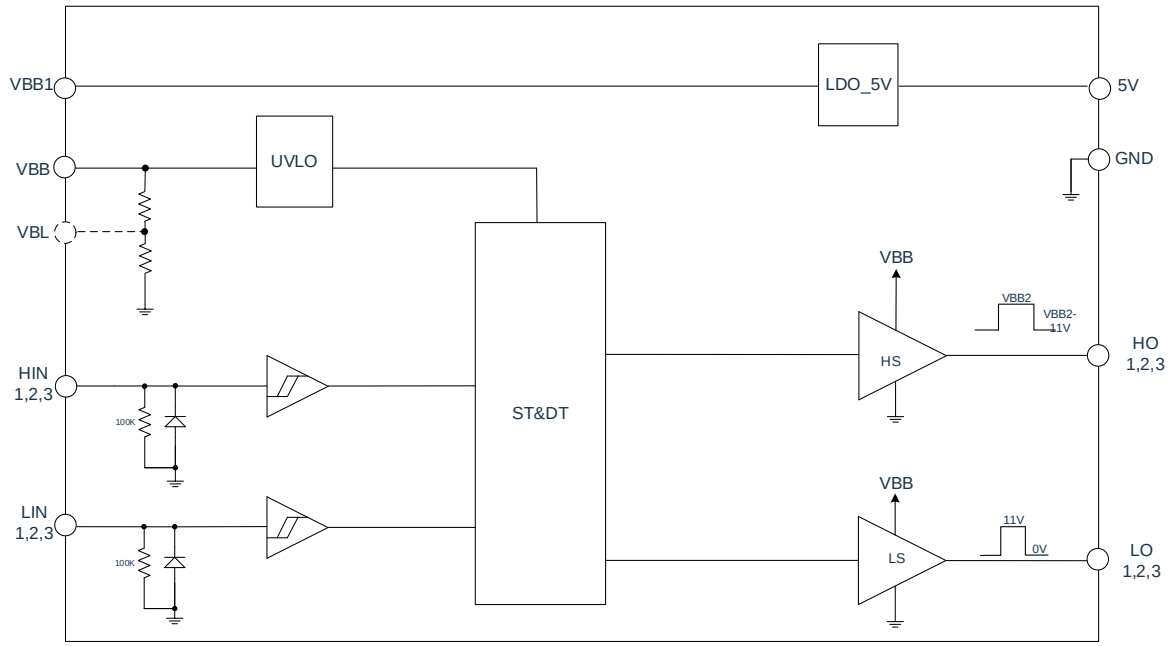
PMOS Logical Truth Table

P*_IN	P*_OUT
Hanging	H
L	H
H	L

Note: *Represents the numbers 1, 2, 3

6.9 GATE DRIVER(3P3N) Electrical Characteristic (CMS32M5526)

6.9.1 Internal Logic Block Diagram



3P3N pre-driver internal logic block diagram

Logic Truth Table

HIN	LIN	UVLO/ST	HO	LO
0	0	0	OFF	OFF
0	1	0	OFF	ON
1	0	0	ON	OFF
1	1	1	OFF	OFF
Hanging	Hanging	0	OFF	OFF

Note:

1) 1: logic high level, 0：logic low level;

2) ON: $V_{HO}=V_{BB}$-11V, V_{LO}=11V OFF：$V_{HO}=V_{BB}$, V_{LO}=0V

6.9.2 Absolute Maximum Ratings

(T_A=25℃, Unless otherwise indicated, GND as a reference point for all pins)

Parameter	Symbol	Value	Unit
5V power supply voltage	V_{BB1}	40	V
Drive power supply voltage	V_{BB}	40	V
LDO output voltage	V_{5V}	6	V
LDO output current	I_{5V}	100	mA
Input voltage (HIN1,2,3/LIN1,2,3)	V_{IN}	10	V
Output voltage of upper half bridge	V_{HO}	12	V
Output voltage of lower half bridge	V_{LO}	12	V
Maximum power consumption (note 1)	P_D	1.4	W
Environmental thermal resistance	θ_{JA}	89	℃/W
Junction temperature	T_J	150	℃
Storage temperature	T_S	-55~+150	℃
Welding temperature of pins (duration 10s)	T_L	260	℃
ESD (note 2)		2000	V

Note：

1) In any case, don't over P_D, the calculation formula of maximum power dissipation under different environmental tempera: $P_D=(150℃-T_A)/\theta_{JA}$
   T_A is the environmental temperature, θ_{JA} is package thermal resistance, the highest junction temperature for the circuit is 150℃;
2) Human model, 100pF capacitor is discharged through the 1.5KΩ resistor;
3) When the working conditions of circuit exceed the range specified by the absolute maximum ratings, it is likely to cause immediate damage to the circuit.

6.9.3 Recommended working conditions

(T_A=25℃, Unless otherwise indicated, GND as a reference point for all pins)

Parameter	Symbol	Min	Typical	Max	Unit
5V power supply voltage	V_{BB1}	9	24	36	V
Drive power supply voltage	V_{BB}	9	24	36	V
Input voltage (HIN/LIN)	V_{IN}	0	-	5	V
Range of working temperature (note 1)	T_{opr}	-20	-	+85	℃

Note：

1) T_{opr} means the environmental temperature of the circuit；
2) Working outside the recommended conditions for a long time may affect its reliability, it is not recommended that the chip work beyond the recommended working conditions for a long time.

6.9.4 Electrical Characteristic parameter table

(TA=25℃, VBB1=VBBB2=24V, GND=0 Unless otherwise indicated)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Power supply current parameters						
V_{BB} static current	I_{VBBQ}	V_{HIN}=V_{LIN}=0	-	660	-	μA
V_{BB} dynamic current	I_{VBBD}	f_{LIN}=16kHz	-	4	-	mA
Power supply voltage parameters						
V_{BB} undervoltage high-level potential	V_{BBHY+}		-	9		V
V_{BB} undervoltage high-level potential	V_{BBHY-}		-	8.5		V
V_{BB} undervoltage hysteresis level	V_{BBHY}		-	0.5	-	V
Input parameters						
Input high level current	I_{IN+}	V_{HIN} 或 V_{LIN}=5V	-	50		μA
Input low level current	I_{IN-}	V_{HIN} 或 V_{LIN}=0	-	0	1	μA
Input high level potential	V_{IN+}		2.5	-	-	V
Input low level potential	V_{IN-}		-	-	0.8	V
Input hysteresis level	V_{INHY}		-	0.8	-	V
Output parameters						
HO output current	I_{HO+}	V_{HIN}=0, V_{HO}=V_{BB}, PWD≤10μs	-	0.4	-	A
HO inhalation current	I_{HO-}	V_{HIN}=5V, V_{HO}=V_{BB}-11V, PWD≤10μs		0.2		A
LO output current	I_{LO+}	V_{LIN}=5V, V_{LO}=0 , PWD≤10μs	-	0.1	-	A
LO inhalation current	I_{LO-}	V_{LIN}=0, V_{LO}=11V , PWD≤10μs		0.3		A
HO output voltage	V_{HO}		V_{BB}-11		V_{BB}	
LO output voltage	V_{LO}	V_{LIN}=5V		11		
Time parameters						
Output rising edge transmission time	T_{ON}	NO Load	-	150	-	ns
Output falling edge transmission time	T_{OFF}	NO Load	-	150	-	ns
HO output rising time	T_{rise_H}	C_L=1nF	-	40	-	ns
HO output falling time	T_{fall_H}	C_L=1nF	-	80	-	ns
LO output rising time	T_{rise_L}	C_L=1nF		150		
LO output falling time	T_{fall_L}	C_L=1nF		55		
Dead time	DT	NO Load	-	200	-	ns
High and low side match time	MT	ΔT_{ON} & ΔT_{OFF}	-	-	50	ns
LDO parameter						
Range of output voltage	V_{5V}	V_{BB1}=9V~36V		5		V
LDO output current	I_{5V}	V_{BB1}=9V~36V	-	-	100	mA
Voltage regulation rate	ΔV_O	I_{5V}=100mA , V_{BB1}=9V~36V		5	10	mV
Load regulation rate	ΔV_{OL}	V_{BB1}=24V , I_{5V}=0~100mA			30	mV

6.10 EMC Characteristic

6.10.1 EFT Electrical Characteristics

Symbol	Parameter	Condition	Max.	Unit	level
V_{EFTB}	Fast transient voltage burst limits to beapplied through 0.1uF(capacitance) on VDD and VSS pins to induce a functional disturbance	T_A = + 25 ℃, HSI=64MHz, conforms to IEC 61000-4-4	4000	V	4B

Note: EFT performance is closely related to system design, including power structure, circuit design, the layout, chip configuration and program structure. EFT parameters in above table are internal testing result in CMS, not suitable for all application environments. These parameters are for reference only. System design has influence upon EFT performance. For some special application which needs high EFT performance, please try to avoid interference sources affecting the system when designing. It is suggested to analyze interfering path and optimize design in order to achieve the best anti-interference performance.

6.10.2 ESD Electrical Characteristics

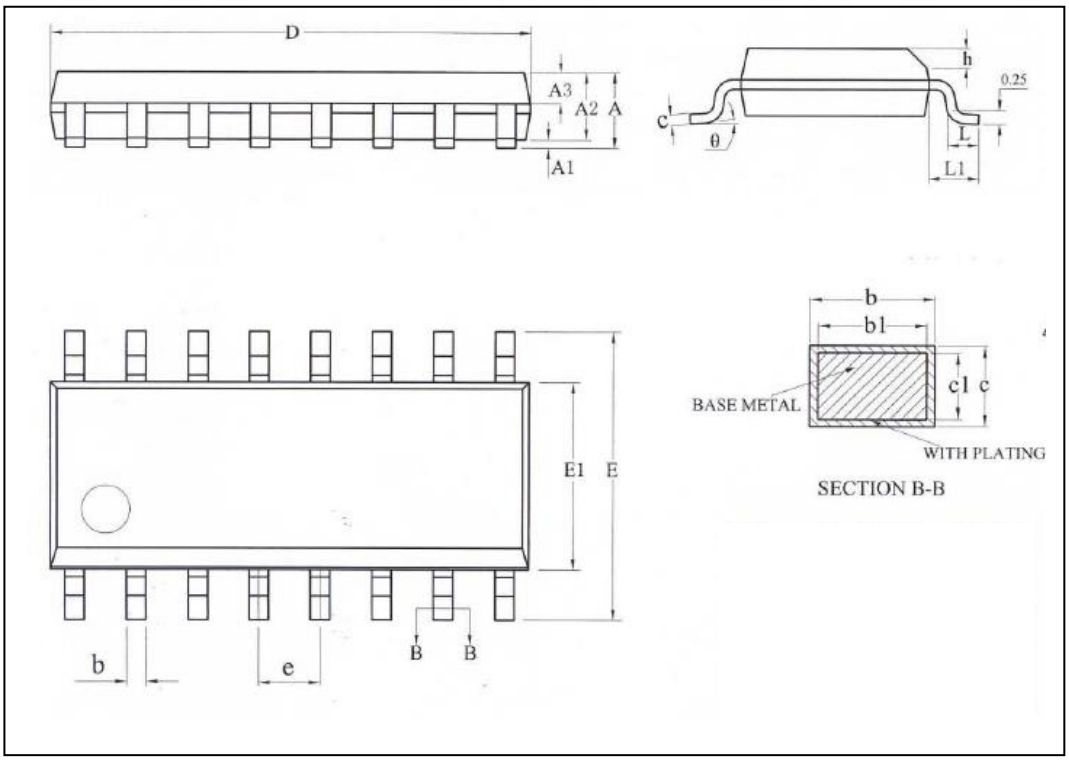
Symbol	Parameter	Condition	Max.	Unit	level
V_{ESD}	Electrostatic discharge (human body model HBM)	T_A = + 25℃, JEDEC EIA/JESD22- A114	8000	V	3B
	Electrostatic discharge (Machine discharge model MM)	T_A = + 25℃, JEDEC EIA/JESD22- A115	400	V	C

6.10.3 Latch-Up Electrical Characteristics

Symbol	Parameter	Condition	Type	Min	Unit
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (TA = +25 ℃)	±200	mA

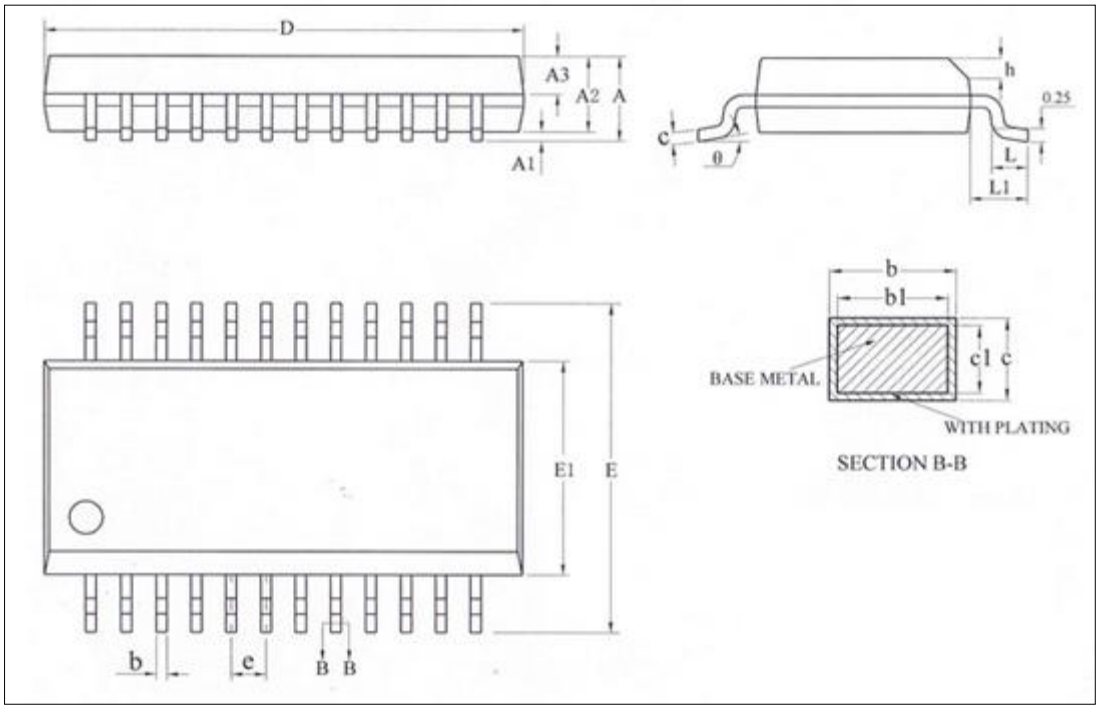
7. Package Dimensions

7.1 SOP16



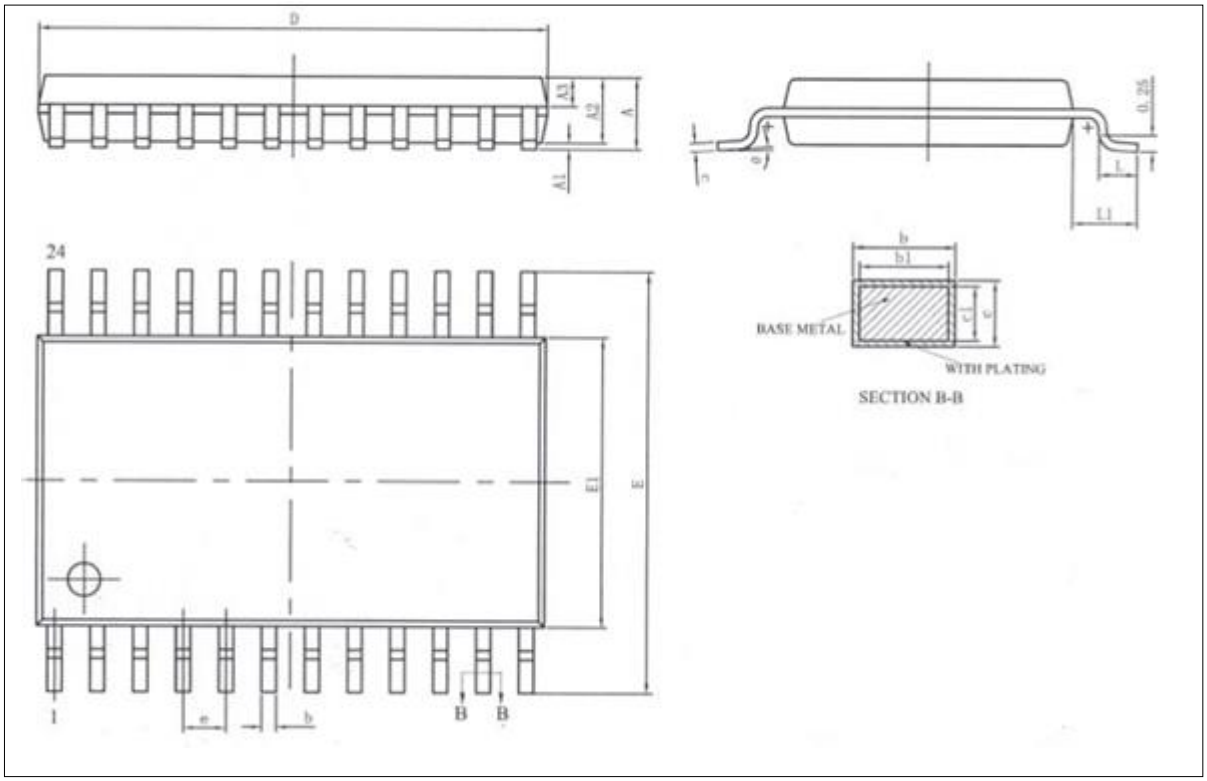
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

7.2 SSOP24



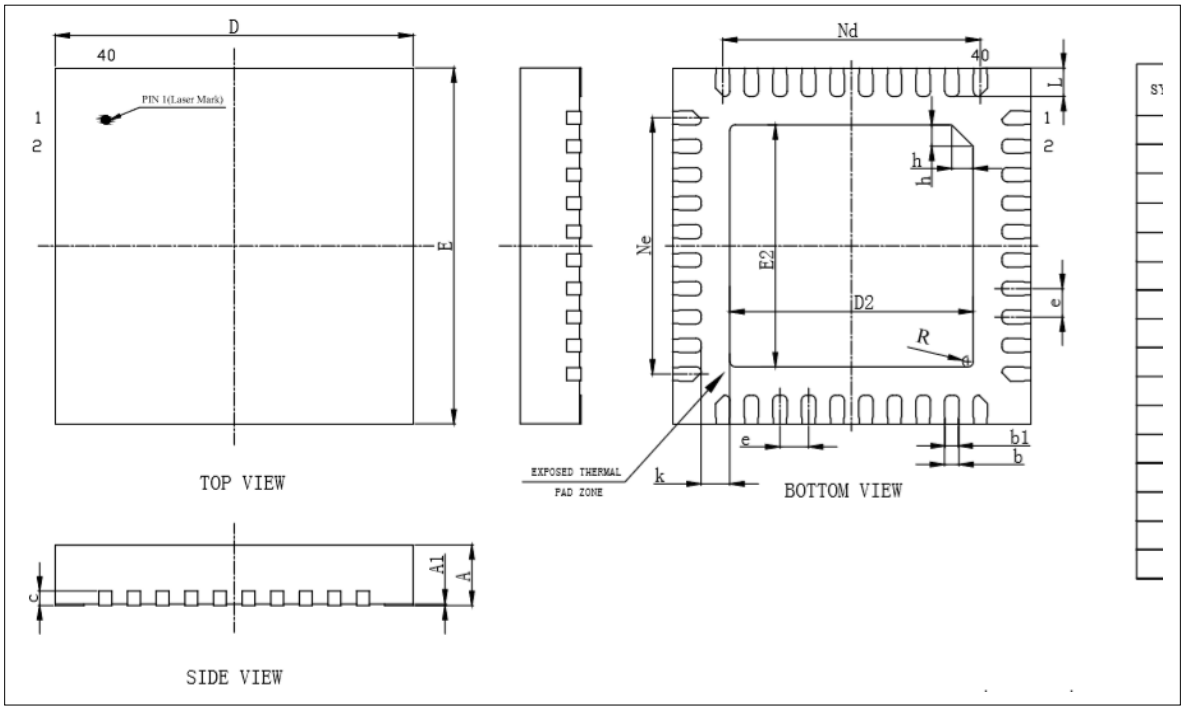
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	-	0.50
L	0.50	-	0.80
L1	1.05REF		
θ	0	-	8°

7.3 TSSOP24



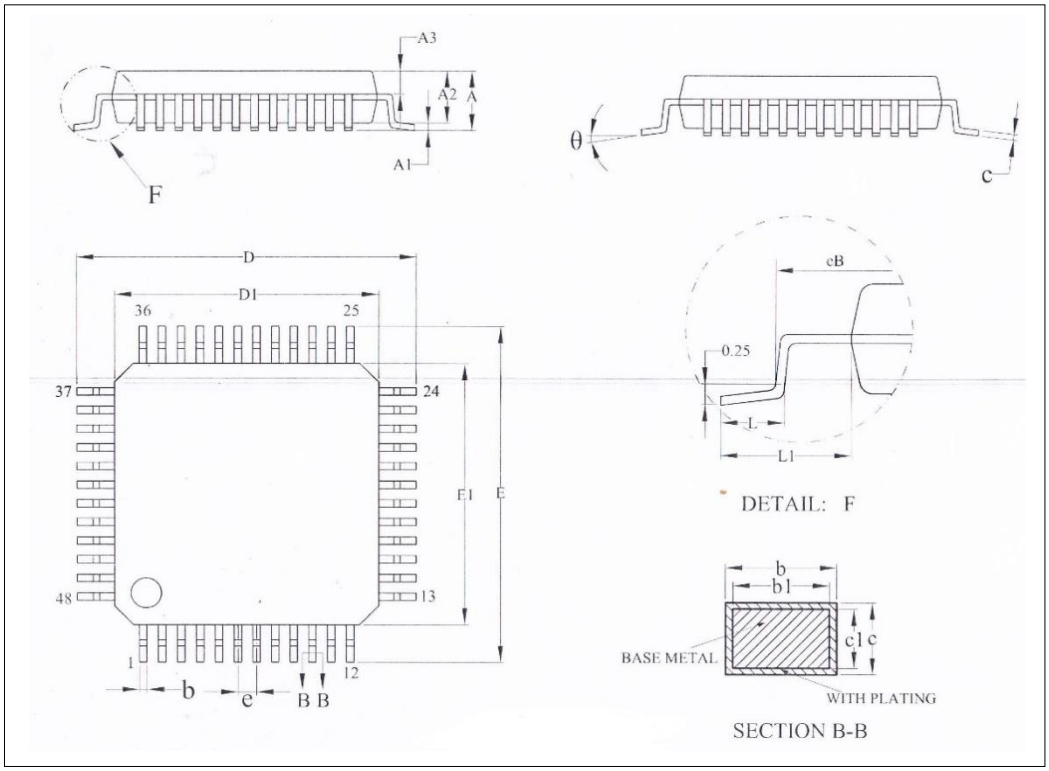
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.2
A1	0.05	-	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.13	-	0.18
c1	0.12	0.13	0.14
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0°	-	8°

7.4 QFN40 (0505X0.85-0.40)



Symbol	Millimeter		
	Min	Nom	Max
A	0.80	0.85	0.9
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.18REF		
c	0.203REF		
D	4.90	5.00	5.10
D2	3.35	3.34	3.45
e	0.40BSC		
Nd	3.60BSC		
Ne	3.60BSC		
E	4.90	5.00	5.10
E2	3.35	3.40	3.45
L	0.35	0.4	0.45
h	0.25	0.30	0.35
R	0.075REF		
k	0.35	0.40	0.45

7.5 LQFP48L (0707X1.4-0.50)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.10	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

8. Ordering Information

Product model	Kernel	Main frequency (MHZ)	Program FLASH (KB)	Data FLASH (KB)	SRAM(KB)	Built-in driver	Built-in LDO	Hardware multiplier	Hardware divider	GPIO	12-Bit ADC0	12-Bit ADC1	Built-in operational amplifier	Built-in PGA	Built-in comparator	EPWM	CCP	Timer	UART	I2C	SPI	Temperature Sensor	CRC	WDT	WWDT	PACKAGE
CMS32M5510S024	M0	64	32	1	8	-	0	1	1	22	22	22	2	2	2	6	2	2	2	1	1	0	1	1	1	SSOP24
CMS32M5512Q040	M0	64	32	1	8	3P3N (8~16V)	0	1	1	22	22	22	2	2	2	6	2	2	2	1	1	0	1	1	1	QFN40
CMS32M5524S016	M0	64	32	1	8	3P3N (16~30V)	0	1	1	7	7	7	1	2	1	6	2	2	1	1	0	0	1	1	1	SOP16
CMS32M5524S024	M0	64	32	1	8	3P3N (16~30V)	0	1	1	14	14	14	2	2	1	6	2	2	2	1	1	0	1	1	1	SSOP24
CMS32M5526TS024	M0	64	32	1	8	3P3N (9~36V)	1	1	1	13	13	13	2	1	1	6	2	2	2	1	1	0	1	1	1	TSSOP24
CMS32M5526S024	M0	64	32	1	8	3P3N (9~36V)	1	1	1	13	13	13	2	1	1	6	2	2	2	1	1	0	1	1	1	SSOP24
CMS32M5526Q040	M0	64	32	1	8	3P3N (9~36V)	1	1	1	23	23	23	2	2	2	6	2	2	2	1	1	0	1	1	1	QFN40
CMS32M5533Q040	M0	64	32	1	8	6N (5.5~18V)	0	1	1	24	24	24	2	2	2	6	2	2	2	1	1	0	1	1	1	QFN40
CMS32M5533L048	M0	64	32	1	8	6N (5.5~18V)	0	1	1	24	24	24	2	2	2	6	2	2	2	1	1	0	1	1	1	LQFP48
CMS32M5536L048	M0	64	32	1	8	6N (8~20V)	0	1	1	24	24	24	2	2	2	6	2	2	2	1	1	0	1	1	1	LQFP48

9. Revision History

Revision	Date	Modify content
V1.00	Apr 2019	Initial version
V1.01	Apr 2020	Modify the description of memory space
V1.02	May 2020	System overview chapter adds system structure block diagram
V1.03	Sep 2020	Add SOP16 pin map and related information of CMS32M5524
V1.04	Oct 2020	Modify the static/dynamic parameters in Chapter 6.8
V1.05	Nov 2020	Add related information of CMS5510S016/CMS5512S016/CMS5336L048
V1.06	Dec 2020	Add related information of CMS32M5533L032
V1.07	Jul 2021	1) Add related information of CMS32M5524TS024/CMS32M5526TS024 2) Remove related information of CMS32M5332/ CMS32M5333L/ CMS32M5510sop16/ CMS32M5512 sop16
V1.08	Sep 2021	1) Add related information of CMS32M5526S024/CMS32M5526Q040 2) Add related information of CMS32M5512
V1.09	Feb 2022	Modify the parameters in Chapter 6.7
V1.10	Apr 2022	1) 3.1 Pin Description, 3.2 Pin functions Description, 3.4 Pin Function List: Adjust SWD pin description and remarks (5) 2) 7.3 TSSOP24: Delete the chip picture
V1.11	Jun 2022	1) Modify the system block diagram of CMS32M5512 in chapter 2.3.2 2) 3.1.2 CMS32M5512(QFN40), 3.1.6CMS32M5526(QFN40), 3.1.7 CMS32M5533(QFN40), 3.1.9 CMS32M5536(LQFP48), 3.2 Pin functions Description, 3.4 Pin Function List: delete CCP0A function of P30
V1.12	Jul 2022	1.2 Product Comparison: add maximum voltage parameters
V1.13	Aug 2022	Corrected the QFN pin map format: 3.1.2 CMS32M5512(QFN40), 3.1.6 CMS32M5526(QFN40), 3.1.7 CMS32M5533(QFN40)