CMS32H3201 Datasheet

Based on ARM® Cortex®-M0+ Ultra Low Power 32bit microcontroller

Built-in 256Kbytes Flash, rich analog function, timers and many types of communication interfaces

Rev 1.13

1 Product Feature

1.1 Features

- **Ultra low power operation enviorment:**
  - Supply voltage range:1.8V to 4.4V
  - Temperature range:-40℃ to 85℃
  - Low power modes: sleep mode, deep sleep mode
  - Operating power consumption: 120uA/MHz@64MHz
  - Power consumption in deep sleep mode: 0.7uA
  - Deep sleep mode+32.768K+RTC:1.2uA
- **Core:**
  - ARM®32-bitCortex®-M0+ CPU
  - Working frequency:32KHz～64MHz
- **Memory:**
  - 256KB Flash memory, with program and data storage shared
  - 2.5KB dedicated data Flash memory
  - 32KB SRAM memory with parity check
  - Support Remap function, you can choose to boot from Boot area, Code Flash area or RAM area
- **Power and reset management:**
  - Built-in power-on reset (POR) circuit
  - Built-in voltage detection (LVD) circuit (threshold voltage can be set)
- **Clock management:**
  - Built-in high-speed vibrator, accuracy (±1%). Can provide 1MHz～64MHz system clock and peripheral module operation clock
  - Built-in 15KHz low-speed oscillator
  - Built-in 2 PLL
  - Support 1MHz～20MHz external crystal oscillator
  - Support 32.768KHz external crystal oscillator
- **Multiplier/divider module:**
  - Multiplier: Support single cycle 32bit multiplication operation
  - Divider: Support 32bit signed integer division operation, only 8 CPU clock cycles to complete an operation
- **Enhanced DMA controller:**
  - Interrupt trigger start.
  - Transmission mode is selectable (normal transmission mode, repeated transmission mode,
- **Input/output port:**
  - Number of I/O port:38～52
  - Can switch between N-channel open drain and internal pull-up and pull-down
  - Built-in button interrupt detection function
  - Built-in clock output/buzzer output control circuit
- **Serial two-wire debugger (SWD)**
- **Rich timers:**
  - 16-bit timer: 12 channels
  - 15-bit interval timer: 1
  - Real-time clock (RTC): 1 (with perpetual calendar, alarm clock function, and supports a wide range of clock correction)
  - Watchdog timer(WWDT):1
  - SysTick timer
- **24bits Sigma-Delta ADC**
  - Built-in LDO
  - Support single path differential input
  - Built-in oscillator
  - Integrated temperature sensor
  - Support sleep mode
  - 2 wire SPI interface, max rate 1.1MHz
  - ADC Features:
    - 24bit lossless code;
    - PGA selectable amplifier:1, 2, 4, 8, 16, 32, 64, 128, 256;
    - Selectable Output rate(ODR):2.5Hz-2.56KHz;
    - While PGA=128, ODR=10Hz, SET_LDO=00, effective resolution is 20.6bits;
    - While PGA=128, ODR=10Hz, SET_LDO=00, equvalent nput noise is 30nVrms.
- **Rich and flexible interfaces:**
  - 3-channel serial communication unit: each channel can be freely configured as a 1-channel standard UART, 2-channel SPI or 2-channel simple I2C
  - Standard SPI:2 channels(support 8bit and16bit)
  - Standard I2C:2 channels
  - I2S:1 channel
  - QSPI:1 channel, support data encryption
  - LCD BUS interface:Support 8080, 6800 interface

block transmission mode and chain transmission mode)
- The transmission source/destination area is optional for the full address space range

- **Linkage controller:**
  - The event signals can be linked together to realize the linkage of peripheral functions.
  - 15 types of event input, 4 types of event trigger.
- **Rich analog peripheral:**
  - 12-bit precision ADC converter, conversion rate 1.42Msps, 28 external analog channels, internal optional PGA0 output as conversion channel, with temperature sensor, support single-channel conversion mode and multi-channel scan conversion mode Conversion range: 0 to positive reference voltage
  - Comparator (CMP), built-in two-channel comparator with hysteresis, optional input source, reference voltage can be external reference voltage or internal reference voltage
  - Programmable gain amplifier (PGA), built-in one channel PGA, can set 1/2/4/8/16/32/64/128 times gain, with external GND pin (can be used as differential mode), output with sample and hold Circuit to support offset voltage trimming
- **USB Interface:**
  - Compatible with USB 2.0 specification
  - Can be used as host controller or device controller
  - Support USB 2.0 full-speed and low-speed transmission
  - Support synchronous transmission, control transmission, batch transmission and interrupt transmission
  - Compatible with USB BC1.2
  - On-The-Go(OTG) feature
- **Safety function:**
  - Comply with relevant standards of IEC/UL 60730
  - Abnormal storage space access error
  - Support RAM parity check
  - Support hardware CRC check
  - Support important SFR protection to prevent misoperation
  - 128-bit unique ID number
  - Flash secondary protection in debug mode (level1: only the entire flash area can be erased, not read or write; level2: the emulator connection is invalid, and the flash operation is not possible)
- **Package:**
  - 64Pin package type

Product model:

Product model	Package	Pin Count
CMS32H3201	64 LQFP(7×7mm, 0.4mm pitch)	64 Pins

FLASH, SRAM size:

Flash Storage	Dedicated Data Flash Storage	SRAM
256KB	2.5KB	32KB

2 System Overview

2.1 System Introduction

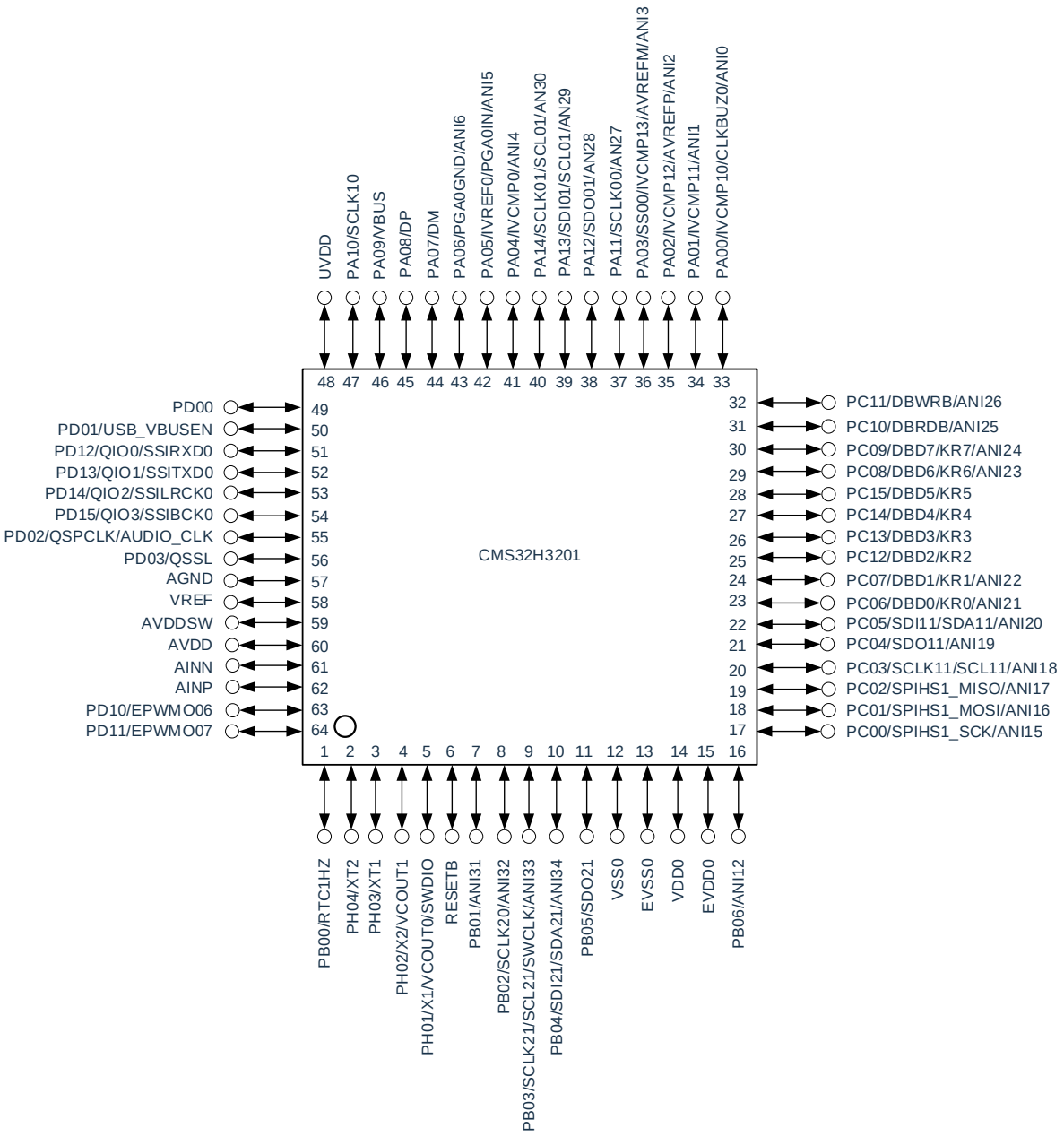
Ultra lower power CMS32H3201 uses high performance ARM®Cortex®-M0+的32 bit RISC core, the max operation rate is 64 Mhz, it integrated high speed embedded flash (SRAM max 32KB, program/data flash max 256KB). The product integrates I2C, SPI, QSPI, UART, LIN, USB, IIS standard interfaces, integrates 12bitA/D convertor, integrates 24 Bit Sigma-delta ADC, temperature sensor, comparator, programmable gain amplifier. Among those,12bitA/Dconvertor can be used to collect the external sensor signals, reduce system design cost. Chip integrates temperature sensor which can realize real time monitoring of external environment. Chip integrates comparator, which supports high speed and low speed working modes, under high speed mode, it can be used to support high speed motor feedback control, wherees under low speed mode, it can be used for battery monitoring. It integrates 12 channels 16-bit timer modules, along with EPWM control circuit, which can be used to implement controller for one DC motor or 2x step motors.

CMS32H3201 also has excellent low power consumption, support sleep and deep sleep mode, the design is flexible. The operating power consumption is 120uA/MHz@64MHz, in deep sleep mode, the power consumption is only 0.7uA, suitable for battery supplied low power devices. At the same time, Leveraging the integrated event linkage controller, which can realize the direct linkage between hardware modules without the needs of CPU intervention, it has faster response compared to using interrupt method, at the same time, it reduces the CPU operation frequency, which prolong the battery life.

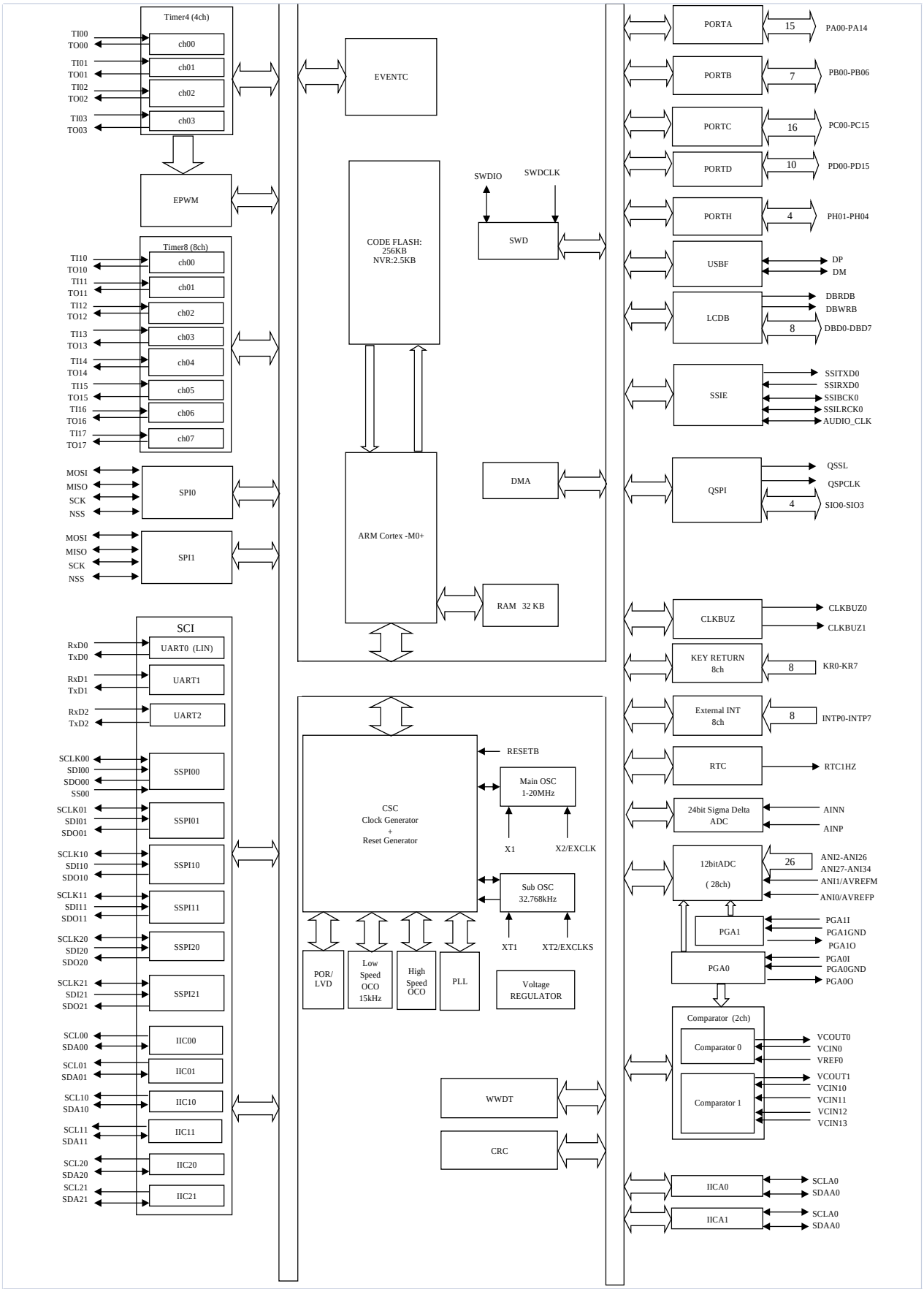
There features make CMS32H3201microcontroller series widely adaptable to consumer products such as home appliance, mobile devices.etc.

2.2 Pin Description

2.2.1 CMS32H3201 Pinout Diagram

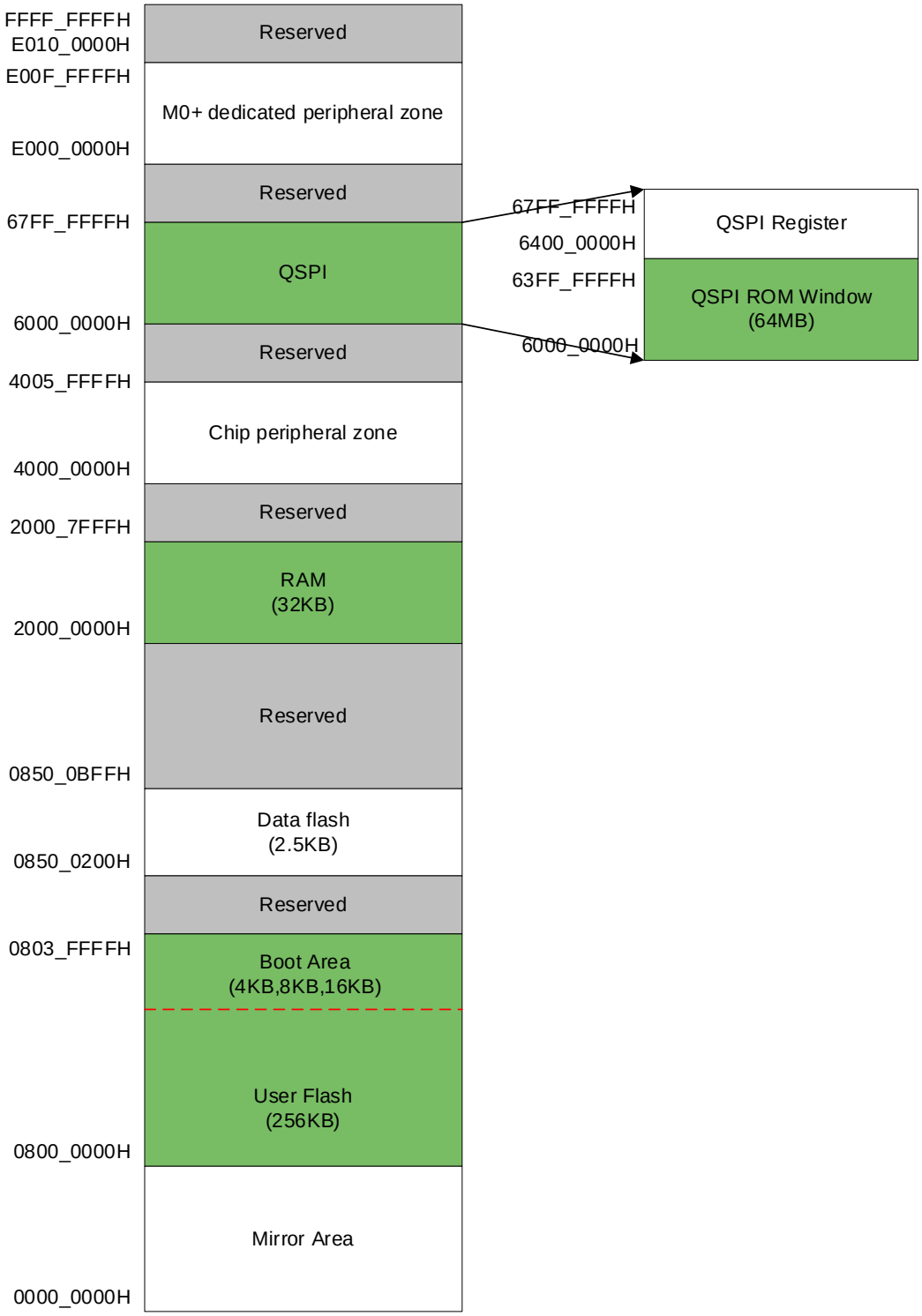


3 Product Structure Diagram



4 Memory Map

Note: Green zone can be remap to mirror zone.



5 Pin Function

5.1 Interface Function

The interface functionalities are shown in below table:

Interface Name	Multiplex function	Digital output function set pxxcfg[3:0]	Digital input function set register xxxPCFG[5:0]
RESETB	RESETB	-	-
PA00	GPIO	00H	00H
	ANI0	00H	00H
	VCIN10	00H	00H
	CLKBUZ0	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA01	GPIO	00H	00H
	ANI1	00H	00H
	VCIN11	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA02	GPIO	00H	00H
	ANI2	00H	00H
	AVREFP	00H	00H
	VCIN12	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA03	GPIO	00H	00H
	ANI3	00H	00H
	AVREFM	00H	00H
	VCIN13	00H	00H
	SS00	00H	00H
	PGA_ADJOUT	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA04	GPIO	00H	00H
	ANI4	00H	00H
	VCIN0	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA05	GPIO	00H	00H
	ANI5	00H	00H
	VREF0	00H	00H
	PGA0IN	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA06	GPIO	00H	00H
	ANI6	00H	00H
	PGA0GND	00H	00H
	Configurable digital function	X(refer to digital function configuration	X(refer to digital function configuration

Interface Name	Multiplex function	Digital output function set pxxcfg[3:0]	Digital input function set register xxxPCFG[5:0]
		overview table)	overview table)
PA07	GPIO	00H	00H
	USB_DM	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA08	GPIO	00H	00H
	USB_DP	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA09	GPIO	00H	00H
	USB_VBUS	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA10	GPIO	00H	00H
	SCLK10	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA11	GPIO	00H	00H
	ANI27	00H	00H
	SCLK00	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA12	GPIO	00H	00H
	ANI28	00H	00H
	SDO01	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA13	GPIO	00H	00H
	ANI29	00H	00H
	SDI01/SDA01	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PA14	GPIO	00H	00H
	ANI30	00H	00H
	SCLK01/SCL01	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PB00	GPIO	00H	00H
	RTC1HZ	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PB01	GPIO	00H	00H
	ANI31	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PB02	GPIO	00H	00H
	ANI32	00H	00H
	SCLK20	00H	00H
	Configurable digital function	X(refer to digital function configuration	X(refer to digital function configuration

Interface Name	Multiplex function	Digital output function set pxxcfg[3:0]	Digital input function set register xxxPCFG[5:0]
		overview table)	overview table)
PB03	GPIO	00H	00H
	ANI33	00H	00H
	SCLK21/SCL21	00H	00H
	SWCLK	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PB04	GPIO	00H	00H
	ANI34	00H	00H
	SDI21/SDA21	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PB05	GPIO	00H	00H
	SDO21	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PB06	GPIO	00H	00H
	ANI12	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC00	GPIO	00H	00H
	ANI15	00H	00H
	SPI1_SCK	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC01	GPIO	00H	00H
	ANI16	00H	00H
	SPI1_MOSI	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC02	GPIO	00H	00H
	ANI17	00H	00H
	SPI1_MISO	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC03	GPIO	00H	00H
	ANI18	00H	00H
	SPI0_SCK	00H	00H
	SCLK11/SCL11	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC04	GPIO	00H	00H
	ANI19	00H	00H
	SPI0_MOSI	00H	00H
	SDO11	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC05	GPIO	00H	00H
	ANI20	00H	00H

Interface Name	Multiplex function	Digital output function set pxxcfg[3:0]	Digital input function set register xxxPCFG[5:0]
	SPI0_MISO	00H	00H
	SDI11/SDA11	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC06	GPIO	00H	00H
	ANI21	00H	00H
	KR0	00H	00H
	DBD0	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC07	GPIO	00H	00H
	ANI22	00H	00H
	KR1	00H	00H
	DBD1	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC08	GPIO	00H	00H
	ANI23	00H	00H
	KR6	00H	00H
	DBD6	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC09	GPIO	00H	00H
	ANI24	00H	00H
	KR7	00H	00H
	DBD7	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC10	GPIO	00H	00H
	ANI25	00H	00H
	DBRDB	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC11	GPIO	00H	00H
	ANI26	00H	00H
	DBWRB	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC12	GPIO	00H	00H
	DBD2	00H	00H
	KR2	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC13	GPIO	00H	00H
	DBD3	00H	00H
	KR3	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC14	GPIO	00H	00H

Interface Name	Multiplex function	Digital output function set pxxcfg[3:0]	Digital input function set register xxxPCFG[5:0]
	DBD4	00H	00H
	KR4	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PC15	GPIO	00H	00H
	DBD5	00H	00H
	KR5	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PD00	GPIO	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PD01	GPIO	00H	00H
	USB_VBUSEN	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PD02	GPIO	00H	00H
	QSPCLK	00H	00H
	SSIMCLK	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PD03	GPIO	00H	00H
	QSSL	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
AGND	AGND	-	-
VREF	Reference input, shall not higher than AVDDSW interface voltage	-	-
AVDDSW	Internal LDO output, External connect to >1uF Capacitor	-	-
AVDD	Power supply	-	-
AINN	Channel negative input	-	-
AINP	Channel positive input	-	-
PD10	GPIO	00H	00H
	EPWMO06	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PD11	GPIO	00H	00H
	EPWMO07	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PD12	GPIO	00H	00H
	QIO0	00H	00H
	SSIRXD0	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PD13	GPIO	00H	00H
	QIO1	00H	00H

Interface Name	Multiplex function	Digital output function set pxxcfg[3:0]	Digital input function set register xxxPCFG[5:0]
	SSITXD0	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PD14	GPIO	00H	00H
	QIO2	00H	00H
	SSIRCK0/SSIFS	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PD15	GPIO	00H	00H
	QIO3	00H	00H
	SSIBCK0	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PH01	GPIO	00H	00H
	X1	00H	00H
	VCOUT0	00H	00H
	SWDIO	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PH02	GPIO	00H	00H
	X2	00H	00H
	EXCLK	00H	00H
	VCOUT1	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PH03	GPIO	00H	00H
	XT1	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
PH04	GPIO	00H	00H
	XT2	00H	00H
	EXCLKS	00H	00H
	Configurable digital function	X(refer to digital function configuration overview table)	X(refer to digital function configuration overview table)
VDD	Power Supply	-	-
VSS	Ground	-	-
UVDD	Power Supply	-	-
UVBUS	Power Supply	-	-
PD8	SCLK, AD clock pin (internal AD pin, does not required external connection)	00H	00H
PD9	DRDYB/DOUT, AD data pin(internal AD pin, does not required external connection)	00H	00H

This product split the 52 ports into GRP0, GRP1, GRP2 groups via digital function configuration, within the group, it is flexible to re-direct some multiplex function. The port grouping and digital function configuration is shown as following.

The 17 ports in GRP0 can be re-direct to channel 0 ~ channel 3 of general timer Timer 4, serial interface UART0 and serial interface IICA0 besides the default multiplex function.

The 20 ports in GRP1 can be re-direct to channel 0 ~ channel 3 of general timer Timer 8, serial interface UART1 and high-speed serial interface SPIHS0 besides the default multiplex function.

The 15 ports in GRP2 can be re-direct to channel 4 ~ channel 7 of general timer Timer 8, serial interface UART2, serial interface IICA1 and buzzer output CLKBUZ1 besides the default multiplex function.

Port Grouping

ID	GRP0	GRP1	GRP2
0	PB00	PC03	PB01
1	PH04	PC04	PB02
2	PH03	PC05	PB03
3	PH02	PC06	PB04
4	PH01	PC07	PB05
5	PC14	PC12	PB06
6	PC15	PC13	-
7	PC08	PA04	-
8	PC09	PA05	PC00
9	PC10	PA06	PC01
10	PC11	PA07	PC02
11	PA00	PA08	PA11
12	PA01	PA09	PA12
13	PA02	PA10	PA13
14	PA03	PD00	PA14
15	-	PD01	PD02
16	-	PD12	PD03
17	-	PD13	-
18	PD10	PD14	-
19	PD11	PD15	-

Digital Function Configuration Overview Table(1/2 Output Function Configuration)

Pin	Control Register	Register Configuraiton	Pin alternative function
GRP0	PB00CFG/PH04CFG/PH03CFG/PH02CFG/ PH01CFG/PC14CFG/PC15CFG/PC08CFG/ PC09CFG/PC10CFG/PC11CFG/PA00CFG/ PA01CFG/PA02CFG/PC03CFG/ PF10CFG/PD11CFG	4'h00	GPIO/Default multiplex Output
		4'h01	TO00
		4'h02	TO01
		4'h03	TO02
		4'h04	TO03
		4'h05	SDO00/TxD0
		Others	Forbidden to use
GRP1	PC03CFG/PC04CFG/PC05CFG/PC06CFG/ PC07CFG/PC12CFG/PC13CFG/PA04CFG/ PA05CFG/PA06CFG/PA07CFG/PA08CFG/ PA09CFG/PA10CFG/PD00CFG/PD01CFG/ PD12CFG/PD13CFG/PD14CFG/PD15CFG	4'h00	GPIO/Default Alternative Output
		4'h01	TO10
		4'h02	TO11
		4'h03	TO12
		4'h04	TO13
		4'h05	TxD1/SDO10
		4'h06	SPIHS0_SCKO
		4'h07	SPIHS0_MO
		4'h08	SPIHS0_SO
		Others	Forbidden to use
GRP2	PB01CFG/PB02CFG/PB03CFG/PB04CFG/ PB05CFG/PB06CFG/ PC00CFG/PC01CFG/PC02CFG/PA11CFG/ PA12CFG/PA13CFG/PA14CFG/PD02CFG/ PD03CFG	4'h00	GPIO/Default Alternative Output
		4'h01	TO14
		4'h02	TO15
		4'h03	TO16
		4'h04	TO17
		4'h05	TxD2/SDO20
		4'h06	CLKBUZ1
		Others	Forbidden to use

Digital Function Configuration Overview Table(2/2 Input Function Configuration)

Pin	Control Register	Register Configuraiton	Pin alternative function
GRP0	TI00PCFG TI01PCFG TI02PCFG TI33PCFG RXD0PCFG(UART) SCLA0PCFG(IICA0) SDAA0PCFG(IICA1)	6'h00	Default Alternative Input
		6'h01	PB00asAlternative Input
		6'h02	PH04asAlternative Input
		6'h03	PH03 as Alternative Input
		6'h04	PH02 as Alternative Input
		6'h05	PH01 as Alternative Input
		6'h06	PC14 as Alternative Input
		6'h07	PC15 as Alternative Input
		6'h08	PC08 as Alternative Input
		6'h09	PC09 as Alternative Input
		6'h0a	PC10 as Alternative Input
		6'h0b	PC11 as Alternative Input
		6'h0c	PA00 as Alternative Input
		6'h0d	PA01 as Alternative Input
		6'h0e	PA02 as Alternative Input
		6'h0f	PA03 as Alternative Input
		6'h10	-
		6'h11	-
		6'h12	-
		6'h13	PD10 as Alternative Input
		6'h14	PD11 as Alternative Input
		Others	Forbidden to use
GRP1	TI10PCFG TI11PCFG TI12PCFG TI13PCFG RXD1PCFG(UART) SPIHS0_SCKIPCFG(SPI) SPIHS0_SIPCFG(SPI) SPIHS0_MIPCFG(SPI)	6'h00	DefaultAlternative Input
		6'h01	PC03 as Alternative Input
		6'h02	PC04 as Alternative Input
		6'h03	PC05 as Alternative Input
		6'h04	PC06 as Alternative Input
		6'h05	PC07 as Alternative Input
		6'h06	PC12 as Alternative Input
		6'h07	PC13 as Alternative Input
		6'h08	PA04 as Alternative Input
		6'h09	PA05 as Alternative Input
		6'h0a	PA06 as Alternative Input
		6'h0b	PA07 as Alternative Input
		6'h0c	PA08 as Alternative Input
		6'h0d	PA09 as Alternative Input
		6'h0e	PA10 as Alternative Input
		6'h0f	PD00 as Alternative Input
		6'h10	PD01 as Alternative Input
		6'h11	PD12 as Alternative Input

Pin	Control Register	Register Configuraiton	Pin alternative function
		6'h12	PD13 as Alternative Input
		6'h13	PD14 as Alternative Input
		6'h14	PD15 as Alternative Input
		Others	Forbidden to use
GRP2	TI14PCFG TI15PCFG TI16PCFG TI17PCFG RXD2PCFG(UART) SPIHS1_NSSPCFG(SPI) SCLA1PCFG(IICA1) SDA1PCFG(IICA1)	6'h00	DefaultAlternative Input
		6'h01	PB01 as Alternative Input
		6'h02	PB02 as Alternative Input
		6'h03	PB03 as Alternative Input
		6'h04	PB04 as Alternative Input
		6'h05	PB05 as Alternative Input
		6'h06	PB06 as Alternative Input
		6'h07	-
		6'h08	-
		6'h09	PC00 as Alternative Input
		6'h0a	PC01 as Alternative Input
		6'h0b	PC02 as Alternative Input
		6'h0c	PA11 as Alternative Input
		6'h0d	PA12 as Alternative Input
		6'h0e	PA13 as Alternative Input
		6'h0f	PA14 as Alternative Input
		6'h10	PD02 as Alternative Input
		6'h11	PD03 as Alternative Input
		6'h12	-
		6'h13	-
		6'h14	-
		Others	Forbidden to use

External interrupt pin function configuration overview table

Pin	Control Register	Register Configuraiton	External Interrupt Port selection
INTP0	INTP0PCFG	3'h00	PC00
		3'h01	PC01
		3'h02	PC02
		3'h03	PC03
		3'h04	PC04
		3'h05	PC05
		3'h06	PC06
		3'h07	PC07
INTP1	INTP1PCFG	3'h00	PC12
		3'h01	PC13
		3'h02	PC14
		3'h03	PC15
		3'h04	PC08
		3'h05	PC09
		3'h06	PC10
		3'h07	PC11
INTP2	INTP2PCFG	3'h00	PA00
		3'h01	PA01
		3'h02	PA02
		3'h03	PA03
		3'h04	PA11
		3'h05	PA12
		3'h06	PA13
		3'h07	PA14
INTP3	INTP3PCFG	3'h00	PA04
		3'h01	PA05
		3'h02	PA06
		3'h03	PA07
		3'h04	PA08
		3'h05	PA09
		3'h06	PA10
		Others	Forbidden to use
INTP4	INTP4PCFG	3'h00	PD00
		3'h01	PD01
		3'h02	PD12
		3'h03	PD13
		3'h04	PD14
		3'h05	PD15
		3'h06	PD02
		3'h07	PD03

Pin	Control Register	Register Configuraiton	External Interrupt Port selection
INTP5	INTP5PCFG	3'h00	-
		3'h01	-
		3'h02	-
		3'h03	-
		3'h04	SCLK(AD clock, requires PD08 related configuration)
		3'h05	DRDYB/DOUT(AD data, requires PD09 related configuration)
		3'h06	PD10
		3'h07	PD11
INTP6	INTP6PCFG	3'h00	PB00
		3'h01	PH04
		3'h02	PH03
		3'h03	PH02
		3'h04	PH01
		3'h05	PB01
		3'h06	PB02
		Others	Forbidden to use
INTP7	INTP7PCFG	3'h00	PB03
		3'h01	PB04
		3'h02	PB05
		3'h03	PB06
		3'h04	-
		3'h05	-
		Others	Forbidden to use

5.2 Port Multiplex Function

(1/2)

Function Name	Input/Output	Function
ANI0～ANI34	Input	A/D Convertor Analog Input
INTP0～INTP7	Input	External Interrupt Request Input Valid Edge selection: Rising Edge, Falling Edge, Rising & Falling edges
VCIN0	Input	Comparator 0 Analog Voltage Input
VCIN10, VCIN11, VCIN12, VCIN13	Input	Comparator 1 Analog Voltage / Reference Voltage Input
VREF0	Input	Comparator 0的 Reference Voltage Input
VCOUT0, VCOUT1	Output	Comparator Output
PGA0IN	Input	PGAInput
PGA0_ADJOUT	Output	PGAOutput
PGA0GND	Input	PGA Reference Input
KR0～KR7	Input	Key interrupt Input
CLKBUZ0, CLKBUZ1	Output	Clock Output/ Buzzer Output
RTC1HZ	Output	Real Time Clock Calibration Clock(1Hz)Output
RESETB	Input	Low voltage valid system reset input, when not used as external reset, must connect direct to VDD via resistor.
RxD0～RxD2	Input	Serial Interface UART0, UART1, UART2 Serial Data Input
TxD0～TxD2	Output	Serial Interface UART0, UART1, UART2 Serial Data Output
SCL00, SCL01, SCL10, SCL11, SCL20, SCL21	Output	Serial Interface IIC00, IIC01, IIC10, IIC11, IIC20, IIC21 Serial Clock Output
SDA00, SDA01, SDA10, SDA11, SDA20, SDA21	Input/Output	Serial Interface IIC00, IIC01, IIC10, IIC11, IIC20, IIC21 Serial Data Input/Output
SCLK00, SCLK01, SCLK10, SCLK11, SCLK20, SCLK21	Input/Output	Serial Interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21 Serial Clock Input/Output
SDI00, SDI01, SDI10, SDI11, SDI20, SDI21	Input	Serial Interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21 Serial Data Input
SS00	Input	Serial Interface SSPI00 chip select Input
SDO00, SDO01, SDO10, SDO11, SDO20, SDO21	Output	SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21 Serial Data Output

(2/2)

Function Name	Input/ Output	Function
SPIHS0_NSS	Input	Serial Interface SPIHS0 Chip Select Input
SPIHS0_SCK	Input/Output	Serial Interface SPIHS0 Serial Clock Input/Output
SPIHS0_MISO	Input/Output	Serial Interface SPIHS0 Serial Data Input/Output
SPIHS0_MOSI	Input/Output	Serial Interface SPIHS0 Serial Data Input/Output
SPIHS1_NSS	Input	Serial Interface SPIHS1 Chip Select Input
SPIHS1_SCK	Input/Output	Serial Interface SPIHS1 Serial Clock Input/Output
SPIHS1_MISO	Input/Output	Serial Interface SPIHS1 Serial Data Input/Output
SPIHS1_MOSI	Input/Output	Serial Interface SPIHS1 Serial Data Input/Output
SCLA0	Input/Output	Serial Interface IICA0的 Clock Input/Output
SDAA0	Input/Output	Serial Interface IICA0 Serial Data Input/Output
SCLA1	Input/Output	Serial Interface IICA1的 Clock Input/Output
SDAA1	Input/Output	Serial Interface IICA1 Serial Data Input/Output
TI00～TI03	Input	16 Bit Timer Timer4 External Counting Clock / Capture Trigger Input
TO00～TO03	Output	16 Bit Timer Timer4 Timer Output
TI10～TI17	Input	16 Bit Timer Timer8 External Counting Clock / Capture Trigger Input
TO10～TO17	Output	16 Bit Timer Timer8 Timer Output
USB_VBUSEN	Output	USBOutput to provide IC的VBUS enable signal of external Power IC
USB_ID	Input	In OTG mode, it connects to IDInput signal of MicroAB connector
USB_EXICEN	Output	Output to OTG Power IC low power control signal
USB_OVRCUA, USB_OVRCUB	Input	Over current Port
USB_DP	Input/Output	USB Transeiver D+ line
USB_DM	Input/Output	USB Transeiver D- line
USB_VBUS	Input	USB connect detection port
UVDD	Input/Output	Input: USB Transeiver power supply, Output: USB LDO Output port.
QIO0~QIO3	Input/Output	QSPI data I/O
QSPCLK	Output	QSPI Clock Output
QSSL	Output	QSPI Slave Selection
SSIRXD0	Input	Serial Audio Interface SSI transimit data
SSITXD0	Output	Serial Audio Interface SSI receive data
SSILRCK0/SSIFS	Input/Output	Serial Audio Interface SSI frame Clock /Frame synchronization
SSIBCK0	Input/Output	Serial Audio Interface SSI bit Clock
SSIMCLK	Input	Serial Audio Interface SSI master Clock
X1, X2	—	Connect to oscillator of main system Clock
EXCLK	Input	External Clock Input of main system Clock
XT1, XT2	—	Connect to oscillator of secondary system Clock
EXCLKS	Input	External Clock Input of secondary system Clock
VDD	—	Power supply
AVREFP	Input	A/D Convertor Positive (+) Reference Voltage Input

Function Name	Input/ Output	Function
AVREFM	Input	A/D Convertor Negative (-) Reference Voltage Input
VSS	—	Ground
SWDIO	Input/Output	SWD data interface
SWCLK	Input	SWD Clock Interface

Remark: As noise and lock strategy, VDD-VSS shall be designed with shortest distance possible and thicker PCB wire shall be used ot connect bypass capacitor (~0.1uF).

6 Functional Overview

6.1 ARM® Cortex®-M0+ Core

ARM's Cortex-M0(+) processor is a new generation of ARM processors for embedded systems. It provides a low-cost platform designed to meet the needs of a small pin count and low-power microcontroller, while providing excellent computing performance and advanced system response to interrupts.

The 32-bit RISC processor of the Cortex-M0(+) processor provides excellent code efficiency and the expected high performance of the ARM core, which is different from 8-bit and 16-bit devices of the same memory size. The Cortex-M0(+) processor has 32 address lines and a storage space of up to 4G.

CMS32H3201 uses an embedded ARM core, so it is compatible with all ARM tools and software.

6.2 Memory

6.2.1 Flash

CMS32H3201 has a built-in flash memory that can be programmed, erased and rewritten. It has the following functions:

- Programs and data share 256K storage space.
- 2.5KB dedicated data Flash memory
- Support page erasing, each page size is 512byte, erasing time 4ms
- Support byte/half-word/word (32bit) programming, programming time 24us

6.2.2 SRAM

CMS32H3201 has built-in 32K bytes of embedded SRAM.

6.3 Enhanced DMA Controller

Built-in enhanced DMA (Direct Memory Access) controller can realize the function of data transfer between memories without using CPU.

- It supports the start of DMA through peripheral function interrupts, and can realize real-time control through communication, timer and A/D.
- The transmission source/destination area is selectable through the entire address space range (when the flash area is used as the destination address, the flash needs to be preset to the programming mode).
- Supports 4 transfer modes (normal transfer mode, repetitive transfer mode, block transfer mode and chain transfer mode).

6.4 Linkage Controller

The linkage controller links each peripheral function output event with the peripheral function trigger source. So as to realize the coordinated operation between peripheral functions without using the CPU.

The linkage controller has the following functions:

- The event signals can be linked together to realize the linkage of peripheral functions.
- 15 types of event input, 4 types of event trigger.

6.5 Clock Generation and Start

The clock generation circuit is a circuit that generates a clock for the CPU and peripheral hardware. There are the following 4 types of system clocks and clock oscillation circuits.

6.5.1 Main System Clock

- X1 oscillator circuit: It can generate 1-20MHz clock oscillation by connecting a resonator to the pins (X1 and X2), and can stop the oscillation by executing a deep sleep command or setting MSTOP.
- High-speed internal oscillator (high-speed OCO): The frequency can be selected for oscillation by the option byte. After the reset is released, the CPU defaults to start running with this high-speed internal oscillator clock. Oscillation can be stopped by executing a deep sleep instruction or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed internal oscillator. The highest frequency is 64Mhz, and the accuracy is ±1.0%.
- Input the external clock from the pin (X2): (1～20MHz), and the input of the external main system clock can be disabled by executing the deep sleep instruction or setting the MSTOP bit.

6.5.2 Secondary System Clock

- XT1 oscillator circuit: It can generate 32.768KHz clock oscillation by connecting a 32.768KHz resonator to the pins (XT1 and XT2), and the oscillation can be stopped by setting the XTSTOP bit.
- Input the external clock from the pin (XT2): 32.768KHz, and the input of the external clock can be disabled by setting the XTSTOP bit.

6.5.3 Low-speed Internal Oscillator Clock

- Low-speed internal oscillator (low-speed OCO): generates 15KHz (TYP.) clock oscillation. The low-speed internal oscillator clock can be used as the CPU clock. The following peripheral hardware can be run by the low-speed internal oscillator clock:
- Watchdog timer(WWDT)
- Real Time Clock(RTC)
- 15-bit interval timer

6.5.4 PLL

- Built-in two PLLs: one is for system clock and the other is for USB. The source clock of the PLL can be either an external clock or a high-speed internal oscillator clock.

6.6 Power Management

6.6.1 Power Supply Mode

VDD: external power supply, voltage range 1.8 to 4.4V.

6.6.2 Power-on Reset

The power-on reset circuit (POR) has the following functions:

- An internal reset signal is generated when the power is turned on. If the power supply voltage (VDD) is greater than the detection voltage (VPOR), the reset is released. However, before reaching the operating voltage range, the reset state must be maintained through a voltage detection circuit or an external reset.
- The power supply voltage (VDD) and the detection voltage (VPDR) are compared. When VDD<VPDR, an internal reset signal is generated. However, when the power supply drops, it must be shifted to the deep sleep mode before it falls below the operating voltage range, or set to the reset state through a voltage detection circuit or an external reset. If you want to restart operation, you must confirm that the power supply voltage has returned to the operating voltage range.

6.6.3 Voltage Detection

The voltage detection circuit sets the operation mode and detection voltage (VLVDH, VLVDL, VLVD) through the option byte. The voltage detection (LVD) circuit has the following functions:

- Compare the power supply voltage (VDD) with the detection voltage (VLVDH, VLVDL, VLVD) and generate an internal reset or interrupt request signal.
- The detection voltage of the power supply voltage (VLVDH, VLVDL, VLVD) can select the detection level by the option byte.
- Can run in deep sleep mode.
- When the power supply rises, before reaching the operating voltage range, the reset state must be maintained through a voltage detection circuit or an external reset. When the power supply drops, it must be transferred to the deep sleep mode before being lower than the operating voltage range, or set to the reset state through a voltage detection circuit or an external reset.
- The operating voltage range varies according to the setting of the user option byte.

6.7 Low Power Modes

CMS32H3201 supports two low-power modes to achieve the best compromise between low power consumption, short startup time, and available wake-up sources:

- Sleep mode: Enter the sleep mode by executing the sleep command. The sleep mode is a mode in which the CPU operating clock is stopped. Before setting the sleep mode, if the high-speed system clock oscillator circuit, high-speed internal oscillator, or subsystem clock oscillator circuit is oscillating, each clock continues to oscillate. Although this mode cannot reduce the operating current to the level of the deep sleep mode, it is an effective mode when you want to restart processing immediately through an interrupt request or when you want to perform intermittent operation frequently.
- Deep sleep mode: Enter the deep sleep mode by executing the deep sleep command. The deep sleep mode is a mode to stop the oscillation of the high-speed system clock oscillation circuit and the high-speed internal oscillator and stop the entire system. Can greatly reduce the operating current of the chip. Because the deep sleep mode can be cancelled by an interrupt request, intermittent operation is also possible. However, in the case of the X1 clock, because it is necessary to ensure the wait time for stable oscillation when releasing the deep sleep mode, if you must start processing immediately with an interrupt request, you must select the sleep mode.

In either mode, the registers, flags, and data memory all retain the contents before the standby mode, and also maintain the status of the output latch and output buffer of the input/output port.

6.8 Reset Function

The following 7 methods to generate a reset signal:

1) Input external reset through RESETB pin.
2) Generate an internal reset through the program runaway detection of the watchdog timer.
3) The internal reset is generated by comparing the power supply voltage of the power-on reset (POR) circuit and the detection voltage.
4) The internal reset is generated by comparing the power supply voltage of the voltage detection circuit (LVD) and the detection voltage.
5) Internal reset due to RAM parity error.
6) Internal reset due to access to illegal memory.
7) Software reset

The internal reset is the same as the external reset. After the reset signal is generated, the program is executed from the addresses written in addresses 0000H and 0001H.

6.9 Interrupt Function

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs and 1 non-maskable interrupt (NMI) input. In addition, the processor also supports multiple internal exceptions.

This product has processed 32 maskable interrupt requests (IRQ) and 1 non-maskable interrupt (NMI). For details, please refer to the corresponding chapters of the user manual. The actual number of interrupt sources varies by product.

6.10 Real Time Clock (RTC)

The real-time clock (RTC) has the following functions.

- Counter with year, month, week, day, hour, minute and second.
- Fixed period interrupt function (period: 0.5 second, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm clock: week, hour, minute)
- 1Hz pin output function
- Support the division of the subsystem clock or the main system clock as the running clock of the RTC
- The real-time clock interrupt signal (INTRTC) can be used as a wake-up from deep sleep mode
- Support a wide range of clock correction functions

Only when the sub-system clock (32.768KHz) or the divided frequency of the main system clock is selected as the running clock of the RTC, the year, month, week, day, hour, minute and second can be counted. When the low-speed internal oscillator clock (15KHz) is selected, only the fixed cycle interrupt function can be used.

6.11 Watchdog Timer

1 channel WWDT, 17bit watchdog timer is set to count operation by option byte. The watchdog timer runs on the low-speed internal oscillator clock (15KHz). The watchdog timer is used to detect program runaway. When a program out of control is detected, an internal reset signal is generated.

The following conditions are judged to be out of control of the program:

- When the watchdog timer counter overflows
- When a 1-bit operation instruction is executed on the enable register (WDTE) of the watchdog timer
- When writing data other than "ACH" to the WDTE register
- When writing data to the WDTE register while the window is closed

6.12 SysTick Timer

This timer is dedicated to the real-time operating system, but it can also be used as a standard down counter.

Its characteristics are: when the 24-bit down counter self-filling capacity counter reaches 0, a maskable system interrupt is generated.

6.13 Timer Timer4/Timer8

This product has a built-in timer unit timer4 with 4-channel 16-bit timer and a timer unit timer8 with 8-channel 16-bit customized timer. Each 16-bit timer is called a "channel", which can be used as an independent timer or combined with multiple channels for advanced timer functions.

For details of each function, please refer to the table below:

Independent channel operation function	Multi-channel linkage operation function
● Interval timer ● Square wave output ● External event counter ● Frequency divider ● Measurement of input pulse interval ● Measurement of the high/low level width of the input signal ● Delay counter	● One-shot pulse output ● PWM output ● Multiple PWM output

6.13.1 Independent Channel Operation Function

The independent channel operation function is a function that can independently use any channel without being affected by the operation mode of other channels. The independent channel operation function can be used in the following modes:

1) Interval timer: Can be used as a reference timer that generates interrupts (INTTM) at regular intervals.
2) Square wave output: Whenever an INTTM interrupt is generated, a flip is triggered, and a square wave with a 50% duty cycle is output from the timer output pin (TO).
3) External event counter: Count the valid edge of the input signal of the timer input pin (TI), and if it reaches the specified number of times, it can be used as an event counter to generate an interrupt.
4) Frequency divider function (only limited to channel 0 of unit 0): divide the input clock of the timer input pin (TI00), and then output from the output pin (TO00).
5) Input pulse interval measurement: start counting at the valid edge of the input pulse signal of the timer input pin (TI) and capture the count value at the valid edge of the next pulse to measure the interval of the input pulse.
6) Measurement of the high/low level width of the input signal: start counting on one edge of the input signal of the timer input pin (TI) and capture the count value on the other edge to measure the high or low level of the input signal Width.
7) Delay counter: start counting at the valid edge of the input signal of the timer input pin (TI) and generate an interrupt after any delay period has elapsed.

6.13.2 Multi-channel linkage Operation Function

Multi-channel linkage operation function can be realized by combining the master channel (the basic timer of the main control cycle) and the slave channel (the timer that follows the master control channel). Multi-channel linkage operation function can be used in the following modes:

1) One-shot pulse output: Use two channels in pairs to generate one-shot pulses that can set the output timing and pulse width arbitrarily.
2) PWM (Pulse Width Modulation) output: Use 2 channels in pairs to generate pulses with a period and duty cycle that can be set arbitrarily.
3) Multiple PWM (Pulse Width Modulation) output: It can generate up to 7 kinds of PWM signals with any duty cycle in a fixed cycle by expanding the PWM function and using 1 master channel and multiple slave channels.

6.13.3 8-bit Timer Operation Function

The 8-bit timer operation function can use the 16-bit timer channel as a function of two 8-bit timer channels. (Only channel 1 and channel 3 can be used)

6.13.4 LIN-bus Supported Function

The timer4 unit can be used to check whether the received signal in LIN-bus communication is suitable for the LIN-bus communication format.

1) Wake-up signal detection: Start counting on the falling edge of the input signal of the UART serial data input pin (RxD) and capture the count value on the rising edge to measure the low-level width. If the low-level width is greater than or equal to a certain fixed value, it is considered as a wake-up signal.
2) Interval field detection: After detecting the wake-up signal, start counting from the falling edge of the input signal of the UART serial data input pin (RxD) and capture the count value on the rising edge to measure the low-level width. If the width of the low level is greater than or equal to a certain fixed value, it is regarded as an interval field.
3) Synchronous field pulse width measurement: After detecting the interval field, measure the low-level width and high-level width of the input signal of the UART serial data input pin (RxD). Calculate the baud rate based on the bit interval of the sync field measured in this way.

6.14 EPWM Output Control Circuit

Use Timer4's PWM output function to control one DC motor or two stepping motors. By cutoff the source CMP0 output, INTP0 input and EVENTC events, the output can be cutoff. Through the setting of the software, you can choose from four types of output those are Hi-Z output, low-level output, high-level output, and forbidden cut-off output.

6.15 15-bit Interval Timer

This product has a built-in 15-bit interval timer, which can generate interrupts (INTIT) at any time interval set in advance, and can be used to wake up the chip from deep sleep mode.

6.16 Clock Output/buzzer Output Control Circuit

The clock output controller is used to provide the clock to the peripheral IC, and the buzzer output controller is used to output the square wave of the buzzer frequency. Clock output or buzzer output is realized by dedicated pins.

6.17 Universal Serial Communication Unit

This product has two built-in universal serial communication units, and each unit has up to 4 serial communication channels. It can realize the communication functions of standard SPI, simple SPI, UART and simple I2C.

6.17.1 3-wire Serial Interface (Simple SPI)

Synchronize data transmission and reception with the serial clock (SCK) output from the master control device.

This is a clock synchronous communication interface that uses 1 serial clock (SCK), 1 sending serial data (SO), and 1 receiving serial data (SI) to communicate with a total of 3 communication lines.

[data transmission and reception]

- 7-bit or 8-bit data length
- Phase control of sending and receiving data
- MSB/LSB priority choice

[clock control]

- Choice of master control or slave
- Phase control of input/output clock
- The transmission cycle generated by the prescaler and the internal counter of the channel
- Maximum transfer rate

Master communication: Max.fCLK/2

Slave communication: Max.fMCK/6

[Interrupt function]

- Transmission Completion interrupt, buffer empty interrupt

[Error detection flag]

- Overflow error

6.17.2 Simple SPI With Slave Chip Select Function

SPI serial communication interface supporting slave chip select input function. This is a clock synchronized communiation interface that composes of 4 lines which are a slave chip select input (SSI), a serial clock (SCK), a sending serial data (SO), and a receiving serial data (SI).

[Data sending and receiving]

- 7-bit or 8-bit data length
- Phase control of sending and receiving data
- MSB/LSB priority choice
- Level setting of sending and receiving data

[clock control]

- Phase control of input/output clock
- The transmission cycle generated by the prescaler and the internal counter of the channel
- Maximum transfer rate

Slave communication: Max.f_{MCK}/6

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt

[Error detection flag]

- Overflow error

6.17.3 UART

This function is asynchronous communication through two lines of serial data transmission (TxD) and serial data reception (RxD). Using these two communication lines to send and receive data asynchronously (using the internal baud rate) with other communication parties according to the data frame (consisting of start bit, data, parity bit and stop bit). Full-duplex UART communication can be realized by using two channels dedicated for transmission (even-numbered channels) and dedicated for reception (odd-numbered channels), and LIN-bus can be supported by combining timer4 units and external interrupts (INTP0).

[Data sending and receiving]

- 7-bit, 8-bit or 9-bit data length
- MSB/LSB priority choice
- Selection of level setting and reverse phase of sending and receiving data
- Additional parity check bit, parity check function
- Additional stop bit, stop bit detection

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt
- Error interrupt caused by framing error, parity error or overflow error

[Error detection flag]

- Frame error, parity error, overflow error

[LIN-bus function]

- Wake-up signal detection
- BF detection
- Measurement of synchronization field, calculation of baud rate

6.17.4 Simple I2C

This function is clock synchronization communication with multiple devices through two lines of serial clock (SCL) and serial data (SDA). Because this simple I2C is designed for single communication with flash memory, A/D converters and other devices, it can only be used as a master device. The start condition and stop condition are the same as the operation control register and must comply with the AC characteristics and be processed by software.

[Data sending and receiving]

- Main control sending, main control receiving (only limited to the main control function of single main control)
- ACK output function, ACK detection function
- 8-bit data length (when sending the address, use the upper 7 bits to specify the address, and use the lowest bit for R/W control)
- Generate start and stop conditions through software

[interrupt function]

- End of transmission interrupt

[Error detection flag]

- ACK error, overflow error

[Functions not supported by simple I2C]]

- Slave sending, slave receiving
- Multi-master control function (arbitration failure detection function)
- Waiting for detection function

6.18 Standard Serial Peripheral Interface SPI

The serial peripheral interface SPI has the following 2 modes:

- Operation idle mode: This is a mode used when serial transmission is not performed, which can reduce power consumption
- 3-wire serial I/O mode: This mode uses 3 lines of serial clock (SCK) and serial data bus (MISO and MOSI) to transmit 8-bit or 16-bit data with multiple devices.

6.19 Standard Serial Interface IICA

The serial interface IICA has the following 3 modes:

- Operation idle mode: This is a mode used when serial transmission is not performed, which can reduce power consumption.
- I2C bus mode (supports multiple masters): This mode uses 2 lines of serial clock (SCLA) and serial data bus (SDAA) to transmit 8-bit data with multiple devices. In line with the I2C bus format, the master device can generate "start condition", "address", "indication of the transfer direction", "data" and "stop condition" for the slave device on the serial data bus. The slave device automatically detects the received status and data through hardware. This function can simplify the I2C bus control part of the application. Because the SCLA pin and SDAA pin of the serial interface IICA are used as open-drain output, the serial clock line and the serial data bus require a pull-up resistor.
- Wake-up mode: In the deep sleep mode, when the extension code or the local station address from the master control device is received, the deep sleep mode can be released by generating an interrupt request signal (INTIICA). Set through the IICA control register.

6.20 Serial Audio Interface SSI

1-channel serial audio interface, which can send and receive audio devices to multiple devices that support different audio data formats:

- Communication mode: master or slave, send and receive (full duplex communication)
- Communication format: I2S format, mono format
- FIFO: 4 bytes * 8 segments transmit or receive FIFO

6.21 QSPI

1 Channel Quad SPI, used to connect SPI compatible interface Serial ROM (non-volatile storage, such as serial FLASH, serial EEPROM or serial eRAM):

- Support extended SPI, Dual SPI, Quad SPI protocol
- Caon be configured into SPI mode 0 and mode 3
- Selectable Address width 8, 16, 24, 32 Bit
- Configurable Timing sequence in order to support various types of serial Flash configuration
- Flash Read function; Support read, Rapid read, Rapid read dual output, Rapid read dual I/O, Rapid read quad Output and Rapid read quad I/O instruction.
- Support various types of Flash instruction and function via flexible software control, including erase, program, ID read and power down control.

6.22 USB

1-channel USB module, compatible with USB 2.0 specification, supports host controller mode, device controller mode and OTG function. The host controller supports full-speed and low-speed transmission, and the device controller supports full-speed transmission. The built-in USB transceiver supports control transfer, synchronous transfer, bulk transfer and interrupt transfer.

It supports a data transmission FIFO with a maximum of 10 pipes, and pipe 0 is the default DCP pipe. According to peripheral and communication requirements, any endpoint number can be configured to pipes 1~9.

Compatible with USB BC1.2 specification.

6.23 LCD BUS Interface

LCD bus interface has following features:

- Support 2 different bus standards: 8080 mode, 6800 mode
- Support 8Bit/16 Bit read/write operation
- Transmission Speed adjustable (max 10Mhz)
- DMA transmission triggered via Internal data transmission enable or external bus access completion
- Support DMA read/write

6.24 Analog-to-digital Converter (ADC)

This product has a built-in 12-bit resolution analog-to-digital converter SARADC, which can convert analog input to digital value and supports up to 28 channels of ADC analog input (ANI0～ANI34). The ADC contains the following functions:

- 12-bit resolution, conversion rate 1.42Msps.
- Trigger mode: support software trigger, hardware trigger and hardware trigger in standby state
- Channel selection: support two modes of single-channel selection and multi-channel scanning
- Conversion mode: support single conversion and continuous conversion
- Working voltage: Support the working voltage range of 1.8V≤VDD≤4.4V
- It can detect the built-in reference voltage (1.45V) and temperature sensor.

ADC can set various A/D conversion modes through the following mode combination

Trigger mode	Software trigger	Start the conversion by software operation.
	Hardware triggers no wait mode	Start the conversion by detecting the hardware trigger.
	Hardware triggers wait mode	In the conversion standby state with the power off, the power is turned on by detecting the hardware trigger, and the conversion starts automatically after the A/D power stabilization wait time.
Channel selection mode	Select mode	Select 1 channel of analog input for A/D conversion.
	Scan mode	Perform A/D conversion on 4 channels of analog input in sequence. It is possible to select 4 consecutive channels from ANI0 to ANI15 as analog input.
Conversion mode	Single conversion mode	Perform 1 A/D conversion on the selected channel.
	Continuous conversion mode	Perform continuous A/D conversion on the selected channel until it is stopped by software.
Sampling time/conversion time	Number of sampling clocks/number of conversion clocks	The sampling time can be set by the register. The default value of the sampling clock is 13.5 clk, and the Min value of the conversion clock is 31.5 clk.

6.25 Sigma-Delta ADC

Sigma-Delta ADC has the following features:

- Built-in LDO
- Support single path diffential Input
- Built-in Oscillator
- Integrated Temperature Sensor
- Support Sleep mode
- 2-wire SPI interface, max rate is 1.1MHz
- ADC Features:
  - 24 Bit lossless code.
  - PGA selectable amplifer gain:1, 2, 4, 8, 16, 32, 64, 128, 256;
  - Selectable Output rate(ODR):2.5Hz-2.56KHz;
  - PGA=128, ODR=10Hz, SET_LDO=00 时, effecive resolution 20.6 Bit;
  - PGA=128, ODR=10Hz, SET_LDO=00 时, equvalent Input noise 30nVrms.

6.26 Programmable Gain Amplifier (PGA)

This product has a built-in programmable gain amplifier (PGA0), which has the following functions:

- Multi-stage gain optional (1/2/4/8/16/32/64/128)
- PGA0 output with sample and hold circuit
- Support offsetted voltage calibration
- Support single-ended/pseudo-differential input
- Support PGA output test.
- PGA output can be connected to internal analog comparator input for shaping.
- The output of PGA0 can be selected as analog input for A/D converter or analog input for positive terminal of comparator0 (CMP0).
- Support offsetted voltage software calibration.

6.27 Comparator (CMP)

This product has built-in two channels with hysteresis comparatorCMP0 and CMP1, with the following functions:

- Can choose comparator high-speed mode, comparator low-speed mode or comparator window mode.
- Can select external reference voltage input and internal reference voltage for reference voltage.
- The elimination width of the noise elimination digital filter can be selected.
- Can detect the valid edge of the comparator output and generate an interrupt signal.
- It can detect the valid edge of the comparator output and output the event signal to the linkage controller.

6.28 Two-wire Serial Debug Port (SW-DP)

ARM's SW-DP interface allows to connect to the microcontroller through a serial wire debugging tool.

6.29 Safety Function

6.29.1 Flash CRC Calculation Function (High-Speed CRC, General-purpose CRC)

Detect the data error of flash memory through CRC operation.

According to different purposes and conditions of use, the following 2 CRCs can be used respectively.

- High-speed CRC: In the initialization program, it can stop the operation of the CPU and check the entire code flash area at high speed.
- General CRC: In CPU operation, it is not limited to the code flash area but can be used for multi-purpose checking.

6.29.2 RAM Parity Error Detection Function

When reading RAM data, detect parity errors.

6.29.3 SFR Protection Function

Prevent the important SFR (Special Function Register) from being rewritten due to CPU out of control.

6.29.4 Illegal Memory Access Detection Function

Detect illegal access to illegal memory area (area without memory or area with restricted access).

6.29.5 Frequency Detection Function

Can use timer4 unit to self-check CPU or peripheral hardware clock frequency.

6.29.6 A/D Test Function

Perform A/D conversion on the A/D converter's positive (+) reference voltage, negative (-) reference voltage, analog input channel (ANI), temperature sensor output voltage, and internal reference voltage Self-test.

6.29.7 Digital Output Signal Level Detection Function of Input/output Port

When the input/output port is in output mode, the output level of the pin can be read.

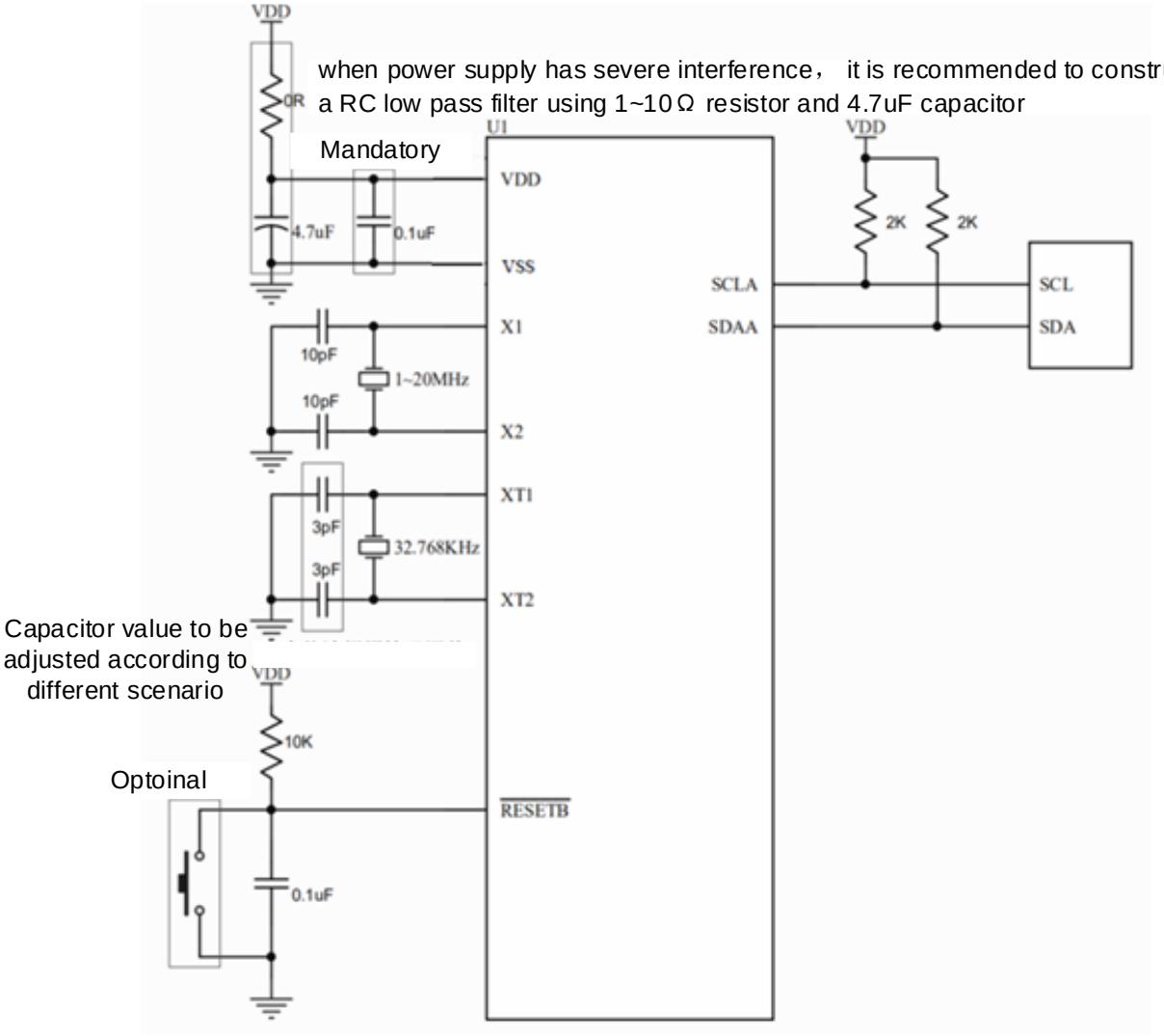
6.30 Key Function

The input pin (KR0～KR7) can be interrupted by the key to generate a key interrupt (INTKR).

7 Electrical characteristics

7.1 Typical Application Peripheral Circuit

The device connection reference of the typical MCU application peripheral circuit is as follows:



7.2 Absolute Maximum Voltage Rating

(T_A=-40～+85°C)

Item	Symbol	Condition	Rating	Unit
Power Voltage	VDD		-0.5～+4.4	V
Input Voltage	VI	PA00～PA14, PB00～PB06, PC00～PC15, PD00～PD15, PH00～PH04, EXCLK, EXCLKS, RESETB	-0.3～VDD+0.3 note1	V
Output Voltage	VO	PA00～PA14, PB00～PB06, PC00～PC15, PD00～PD15, PH01～PH04	-0.3～VDD+0.3 note1	V
Analog Input Voltage	VAI	ANI0～ANI34	-0.3～VDD+0.3 and -0.3～AVREF(+)+0.3 note1, 2	V

NOTE: 1. Not exceeding 4.4V.

2. The pin of the A/D conversion target cannot exceed AVREF (+) +0.3.

Attention: Even if one of the items exceeds the absolute maximum rating for a short period, the quality of the product may be degraded. The absolute maximum rating is a rating that may cause physical damage to the product, and the product must be used under the condition that the rating is not exceeded.

Remarks:

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. AVREF (+): The positive (+) reference voltage of the A/D converter
3. Use VSS as the reference voltage.

7.3 Absolute Maximum Current Rating

(T_A=-40～+85℃)

Item	Symbol	Condition		Rating	Unit
High level output current	IOH1	Each pin	PA00～PA14, PB00～PB06, PC00～PC15, PD00～PD15, PH01～PH04	-40	mA
		Total pins-170mA	PB00～PB06, PD00～PD15	-70	mA
			PA00～PA14, PC00～PC15	-100	mA
	IOH2	Each pin	PH01～PH04	-3	mA
		Total pins		-15	mA
Low-level output current	IOL1	Each pin	PA00～PA14, PB00～PB06, PC00～PC15, PD00～PD15, PH01～PH04	40	mA
		Total pins 170mA	PB00～PB06, PD00～PD15	100	mA
			PA00～PA14, PC00～PC15	120	mA
	IOL2	Each pin	PH01～PH04	15	mA
		Total pins		45	mA
Working temperature	TA	Normally operation		-40～+85	℃
		When flash programming			
storage temperature	Tstg			-65～+150	℃

Attention: Even if one of the items exceeds the absolute maximum rating for a short period, the quality of the product may be degraded. The absolute maximum rating is a rating that may cause physical damage to the product, and the product must be used under the condition that the rating is not exceeded.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

7.4 Oscillation Circuit Characteristics

7.4.1 X1, XT1 Characteristics

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, VSS=0V)

Item	Resonator	Condition	Min	Typ	Max	Unit
X1 clock oscillation frequency (fx)	Ceramic resonator/crystal resonator	1.8V≤VDD≤4.4V	1.0	-	20.0	MHz
XT1 clock oscillation frequency (fxt)	Crystal resonator	1.8V≤VDD≤4.4V	32	32.768	35	KHz

Note: It only indicates the allowable frequency range of the oscillation circuit. Please refer to the AC characteristics for the command execution time.

Please request the resonator manufacturer to evaluate the implemented circuit and use it after confirming the oscillation characteristics.

7.4.2 Internal Oscillator Characteristics

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, VSS=0V)

Resonator	Condition	Min	Typ	Max	Unit
High-speed internal oscillator clock frequency (fIH)note1,2	-	1.0	-	64.0	MHz
Clock frequency accuracy of high-speed internal oscillator	T_A=-20～+85℃	-1.0	-	+1.0	%
	T_A=-40～-20℃	-1.5note3		+1.5note3	%
Clock frequency of low-speed internal oscillator (fIL)	-	10	15	20	KHz

Note:

1. Select the frequency of the high-speed internal oscillator by the option byte.
2. It only shows the characteristics of the oscillation circuit, please refer to the AC characteristics for the command execution time.
3. Low temperature specification value is guaranteed by design, mass production does not measure low temperature condition.

7.4.3 PLL Oscillator Characteristics

(TA=-40～+85℃, 1.8V≤VDD≤4.4V, VSS=0V)

Resonator	Condition	Min	Typ	Max	Unit
PLLInput frequency note1	-	4.0	-	8.0	MHz
PLL lock time	-	40	-	-	μs
UPLL input frequency	-	4.0	-	8.0	MHz
UPLL lock time	-	40	-	-	μs

Note:1. It only shows the characteristics of the oscillation circuit, please refer to the AC characteristics for the command execution time

7.5 DC Characteristics

7.5.1 Pin Characteristics

(TA=-40～+85℃, 1.8V≤VDD≤4.4V, VSS=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High voltage Level Output current note1	IOH1	PA00～PA06, PA09～PA14, PB00～PB06, PC00～PC15, PD00～PD15 1 pin alone	1.8V≤VDD≤4.4V -40～+85℃	-	-	-12.0note2	mA
		PB00～PB06, PD00～PD15 Total pins(duty cycle≤70%note3)	4.0V≤VDD≤4.4V -40～+85℃	-	-	-60.0	mA
			2.4V≤VDD＜4.0V	-	-	-12.0	mA
			1.8V≤VDD＜2.4V	-	-	-6.0	mA
		PA00～PA14, PC00～PC15 Total pins(duty cycle≤70%note3)	4.0V≤VDD≤4.4V -40～+85℃	-	-	-80.0	mA
			2.4V≤VDD＜4.0V	-	-	-20.0	mA
			1.8V≤VDD＜2.4V	-	-	-10.0	mA
		Total pins(duty cycle≤70%note3)	1.8V≤VDD≤4.4V -40～+85℃	-	-	-140.0	mA
	IOH2	PH01～PH04 1 pin alone	1.8V≤VDD≤4.4V	-	-	-2.5note2	mA
		Total pins(duty cycle≤70%note3)	1.8V≤VDD≤4.4V	-	-	-10	mA

Note:

1) This is the current value that guarantees the operation of the device even if current flows from the VDD pin to the output pin.
2) Can not exceed the total current value.
3) This is the output current value of "duty cycle≤70%condition".

   To change the output current value with a duty cycle> 70% can be calculated with the following calculation formula (when the duty cycle is changed to n%).

   - The total output current of the pins = (IOH×0.7)/(n×0.01)

     ＜example＞ IOH =-10.0mA, n =80%

   The total output current of the pins = (-10.0×0.7)/(80×0.01) ≈ -8.7mA

   The current of each pin does not change due to the duty cycle, and no current above the absolute maximum rating will flow.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, VSS=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Low-level output current[note 1]	IOL1	PA00～PA14, PB00～PB08, PC00～PC15, PD00～PD15 1 pin alone	1.8V≤VDD≤4.4V -40～+85℃	-	-	35[note2]	mA
		PB00～PB06, PD00～PD15 Total pins(duty cycle≤ 70%[note3])PB00～PB08, PD00～PD15 Total pins (when duty cycle ≤70%[note3])	4.0V≤VDD≤4.4V -40～+85℃	-	-	100	mA
			2.4V≤VDD＜4.0V	-	-	30	mA
			1.8V≤VDD＜2.4V	-	-	15	mA
		PA00～PA14, PC00～PC15 Total pins (duty cycle≤70%[note3])	4.0V≤VDD≤4.4V -40～+85℃	-	-	120	mA
		PA00～PA14, PC00～PC15 Total pins (when duty cycle ≤70%[note3])	2.4V≤VDD＜4.0V	-	-	40	mA
			1.8V≤VDD＜2.4V	-	-	20	mA
		Total pins(duty cycle≤70%[note3])	1.8V≤VDD≤4.4V -40～+85℃	-	-	150	mA
	IOL2	PH01～PH04 have a single pin	1.8V≤VDD≤4.4V	-	-	10[note2]	mA
		Total pins(duty cycle≤70%[note3])	1.8V≤VDD≤4.4V	-	-	40	mA

Note:

1) This is the current value that guarantees the operation of the device even if the current flows from the output pin to the VSS pin.
2) Can not exceed the total current value.
3) This is the output current value of "duty cycle≤70% condition".
   The output current value with a duty cycle> 70% can be calculated with the following calculation formula (when the duty cycle is changed to n%)
   - The total output current of the pins = (IOL×0.7)/(n×0.01)
     ＜example＞ IOL= 10.0mA, n = 80%

   The total output current of the pins = (10.0×0.7)/(80×0.01) ≈ 8.7mA
   The current of each pin does not change due to the duty cycle, and no current above the absolute maximum rating will flow.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, VSS=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High-level input voltage	VIH1	PA00～PA14, PB00～PB06, PC00～PC15, PD00～PD15, PH00～PH04, EXCLK, EXCLKS, RESETB	Schmidt input	0.8VDD	-	VDD	V
Low-level input voltage	VIL1	PA00～PA14, PB00～PB06, PC00～PC15, PD00～PD15, PH00～PH04, EXCLK, EXCLKS, RESETB	Schmidt input	0	-	0.2VDD	V

Note: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

(T_A=-40 ～ +85℃, 1.8V≤VDD≤4.4V, VSS=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High level output voltage	VOH1	PA00～PA14, PB00～PB06, PC00～PC15, PD00～PD15	4.0V≤VDD≤4.4V, IOH1=-12.0mA	VDD-1.5	-	-	V
			4.0V≤VDD≤4.4V, IOH1=-6.0mA	VDD-0.7	-	-	V
			2.4V≤VDD≤4.4V, IOH1=-3.0mA	VDD-0.6	-	-	V
			1.8V≤VDD≤4.4V, IOH1=-2mA	VDD-0.5	-	-	V
	VOH2	PH01～04	4.0V≤VDD≤4.4V, IOH2=-2.5mA	VDD-1.5	-	-	V
			4.0V≤VDD≤4.4V, IOH2=-1.5mA	VDD-0.7	-	-	V
			2.4V≤VDD≤4.4V, IOH2=-0.5mA	VDD-0.6	-	-	V
			1.8V≤VDD≤4.4V, IOH2=-0.4mA	VDD-0.5	-	-	V
Low-level output voltage	VOL1	PA00～PA14, PB00～PB06, PC00～PC15, PD00～PD15	4.0V≤VDD≤4.4V, IOL1=35.0mA	-	-	1.2	V
			4.0V≤VDD≤4.4V, IOL1=20.0mA	-	-	0.7	V
			2.4V≤VDD≤4.4V, IOL1=9.0mA	-	-	0.4	V
			1.8V≤VDD≤4.4V, IOL1=6.0mA	-	-	0.4	V
	VOL2	PH01～04	4.0V≤VDD≤4.4V, IOL2=10.0mA	-	-	1.2	V
			4.0V≤VDD≤4.4V, IOL2=6.0mA	-	-	0.7	V
			2.4V≤VDD≤4.4V, IOL2=2.5mA	-	-	0.4	V
			1.8V≤VDD≤4.4V, IOL2=1.5mA	-	-	0.4	V

Note: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, VSS=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
High-level input leakage current	ILIH1	PA00～PA14, PB00～PB06, PC00～PC15, PD00～PD15, PH00	VI=VDD	-	-	1	μA
	ILIH2	RESETB	VI=VDD	-	-	1	μA
	ILIH3	PH01～04 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	VI=VDD, when input port and external clock input	-	-	1	μA
			VI=VDD, when the resonator is connected	-	-	10	μA
Low-level input leakage current	ILIL1	PA00～PA14, PB00～PB06, PC00～PC15, PD00～PD15, PH00	VI=VSS	-	-	-1	μA
	ILIL2	RESETB	VI=VSS	-	-	-1	μA
	ILIL3	PH01～04 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	VI=VSS, when input port and external clock input	-	-	-1	μA
			VI=VSS, when the resonator is connected	-	-	-10	μA
Internal pull-up resistor	RU	PA00～PA06, PA10～PA14, PB00～PB06, PC00～PC15, PD00～PD15, PH00～PH02	VI=VSS, when input port	10	30	100	KΩ
Internal pull-down resistor	RD	PA00～PA06, PA09～PA14, PB00～PB06, PC00～PC15, PD00～PD15	VI=VDD, when input port	10	30	100	KΩ

Note: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

7.5.2 Power Supply Current Characteristics

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, V_{SS}=0V)

Item	Symbol	Condition				Min	Typ	Max	Unit
Power supply current note1	I_{DD1}	Operating mode	High-speed internal oscillator	f_{HOCO}=64MHz, f_{IH}=64MHz note3		-	7.6	12.5	mA
				f_{HOCO}=32MHz, f_{IH}=32MHz note3		-	5.8	7.8	
			High-speed main system clock	f_{MX}=20MHz note2	Input方波	-	4.0	5.2	mA
					Connect the crystal	-	4.0	5.2	
			Secondary clock running	f_{SUB}=32.768KHz note4	Input方波	-	70	85	uA
					Connect the crystal	-	70	85	
			Low-speed internal oscillator	fIL=15KHz note8		-	70	85	uA
	I_{DD2}	Sleep mode	High-speed internal oscillator	f_{HOCO}=64MHz, f_{IH}=64MHz note3		-	1.8	7.0	mA
				f_{HOCO}=32MHz, f_{IH}=32MHz note3		-	1.2	3.8	
			High-speed main system clock	f_{MX}=20MHz note2	Input方波	-	0.7	2.5	mA
					Connect the crystal	-	0.7	2.5	
			Subsystem clock running	f_{SUB}=32.768KHz note5	Input方波	-	1.2	14.5	uA
					Connect the crystal	-	1.2	14.5	
			Low-speed internal oscillator	fIL=15KHz note8		-	1.4	15	uA
	I_{DD3} note6	Deep sleep mode note7	T_A=-40℃~+70℃ VDD=3.0V			-	0.7	4.0	uA
			T_A=-40℃~+85℃ VDD=3.0V			-	0.7	7.0	

Note:

1) This is the current flowing through VDD, including the input leakage current when the input pin is fixed to VDD or VSS. TYP. Value: CPU is in the execution of multiplication instruction (IDD1), and does not include peripheral operating current. MAX. Value: CPU is in full instruction execution action (IDD1), and includes peripheral operating current, but does not include the flow to the A/D converter,
the current of the LVD circuit, I/O port, and internal pull-up or pull-down resistors, also does not include the current when modifying data flash memory.
2) This is the case when the high-speed internal oscillator and the subsystem clock stop oscillating.
3) This is the case where the high-speed main system clock and subsystem clock stop oscillating.
4) This is the case when the high-speed internal oscillator and the high-speed main system clock stop oscillating.
5) This is the case when the high-speed internal oscillator and the high-speed main system clock stop oscillating. Contains the current flowing to the RTC, but does not include the 15-bit interval timer and watchdog Timer current
6) Does not include current to RTC, 15-bit interval timer and watchdog timer.

7) For the current value when the subsystem clock is running in the deep sleep mode, please refer to the current value when the subsystem clock is running in the sleep mode.
8) This is the case where the high-speed internal oscillator, the high-speed main system clock and the subsystem clock stop oscillating.

Remarks:

1) fHOCO: The clock frequency of the high-speed internal oscillator, fIH: the system clock frequency provided by the high-speed internal oscillator.
2) fSUB: External secondary clock frequency (XT1/XT2 clock oscillation frequency).
3) fMX: External main system clock frequency (X1/X2 clock oscillation frequency).
4) fIL: Clock frequency of low-speed internal oscillator.
5) TYP. The temperature condition of the value is TA=25°C.

(TA=-40～+85°C, 1.8V≤VDD≤4.4V, VSS=0V)

Parameter	Symbol	Condition		Min.	Typ.	Max	Unit
Low-speed internal oscillator operating current	IFIL note1	-		-	0.2	-	uA
RTC operating current	IRTC note1,2,3	-		-	0.04	-	uA
15-bit interval timer operating current	IIT note1,2,4	-		-	0.02	-	uA
Watchdog timer operating current	IWDT note1,2,5	fIL=15KHz		-	0.22	-	uA
A/D Convertor operating current	IADC note1,6	ADC HS mode @64MHz		-	2.2	-	mA
		ADC HS mode @4MHz		-	1.3	-	mA
		ADC LC mode @24MHz		-	1.1	-	mA
		ADC LC mode @4MHz		-	0.8	-	mA
PGA operating current	IPGA note1,7	Each channel		-	480	700	uA
Comparator operating current	ICMP note1,8	Each channel	Does not use internal reference voltage	-	60	100	uA
			Use internal reference voltage	-	80	140	uA
LVD operating current	ILVD note1,9	-		-	0.08	-	uA

Note:

1) This is the current flowing through VDD.
2) This is the case when the high-speed internal oscillator and the high-speed system clock stop oscillating.
3) This is the current that only flows to the real-time clock (RTC) (not including the operating current of the low-speed internal oscillator and XT1 oscillator circuit). When the real-time clock is running in running mode or sleep mode, the current value of the microcontroller is IDD1 or IDD2 plus the value of IRTC. In addition, when low-speed internal oscillator is selected, IFIL must be added. IDD2 when the subsystem clock is running contains the operating current of the real-time clock.
4) This is the current that only flows to the 15-bit interval timer (not including the operating current of the low-speed internal oscillator and XT1 oscillator circuit). When the 15-bit interval timer is running in run mode or sleep mode, the current value of the microcontroller is the value of IDD1 or IDD2 plus IIT. In

addition, when low-speed internal oscillator is selected, IFIL must be added.

5) This is the current that only flows to the watchdog timer (including the operating current of the low-speed internal oscillator). When the watchdog timer is running, the current value of the microcontroller is IDD1 or IDD2 or IDD3 plus the value of IWDT.
6) This is the current that only flows to the A/D converter. When the A/D converter is running in running mode or sleep mode, the current value of the microcontroller is IDD1 or IDD2 plus the value of IADC.
7) This is the current that only flows to the PGA circuit. When the programmable gain amplifier circuit is running, the current value of the microcontroller is the value of IDD1 or IDD2 or IDD3 plus IPGA.
8) This is the current that only flows to the comparator circuit. When the comparator circuit is running, the current value of the microcontroller is the value of IDD1 or IDD2 or IDD3 plus ICMP.
9) This is the current that only flows to the LVD circuit. In the case of LVD circuit operation, the current value of the microcontroller is the value of IDD1 or IDD2 or IDD3 plus ILVD.

Remark:

1) fIL: Clock frequency of low-speed internal oscillator.
2) TYP. The temperature condition of the value is TA=25℃.

7.6 AC Characteristics

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, V_{SS}=0V)

Iitem	Symbol	Condition		Min	Typ	Max	Unit
Instruction cycle (Minimum instruction execution time)	TCY	Main system clock (fMAIN) running	1.8V≤VDD≤4.4V	0.015625	-	1	μs
		secondary system clock (fSUB) running	1.8V≤VDD≤4.4V	28.5	30.5	31.3	μs
External system clock frequency	fEX	1.8V≤VDD≤4.4V		1.0	-	20.0	MHz
	fEXS	1.8V≤VDD≤4.4V		32.0	-	35.0	KHz
High and low level width of external system clock input	tEXH, tEXL	1.8V≤VDD≤4.4V		24	-	-	ns
	tEXHS, tEXLS	1.8V≤VDD≤4.4V		13.7	-	-	μs
TI00 ～TI03, TI10 ～ TI13, input high and low level width	tTIH, tTIL	1.8V≤VDD≤4.4V		$1/f_{MCK}$+10	-	-	ns
TO00 ～ TO03, TO10 ～ TO13, output frequency	fTO	4.0V≤VDD≤4.4V		-	-	16	MHz
		2.4V≤VDD＜4.0V		-	-	8	MHz
		1.8V≤VDD＜2.4V		-	-	4	MHz
CLKBUZ0, CLKBUZ1 Output frequency	fPCL	4.0V≤VDD≤4.4V		-	-	16	MHz
		2.4V≤VDD＜4.0V		-	-	8	MHz
		1.8V≤VDD＜2.4V		-	-	4	MHz
Interrupt input high and low level width	tINTH, tINTL	INTP0 ～ INTP3	1.8V≤VDD≤4.4V	1	-	-	μs
Key interrupt input high and low level width	tKR	KR0 ～ KR5	1.8V≤VDD≤4.4V	250	-	-	ns
RESETB low-level width	tRSL	-		10	-	-	μs

Remark: fMCK: Operating clock frequency of timer4 unit.

7.7 Peripheral Function Characteristics

7.7.1 Universal Interface Module

1) UART mode

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, V_{SS}=0V)

Item	Condition		Specification Value		Unit
			Min	Max	
Transmission rate	1.8V ≤ VDD ≤ 4.4V	-	-	f_{MCK}/6	bps
		The theoretical value of the maximum transfer rate f_{MCK}=f_{CLK}	-	10.6	Mbps

2) Three-wire SPImode (master mode, internal clock output)

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, V_{SS}=0V)

Item	Symbol	Condition		-40 ～ +85℃		Unit
				Min	Max	
SCLKp Period Time	tKCY1	tKCY1 ≥ 2/f_{CLK}	4.0V ≤ VDD ≤ 4.4V	31.25	-	ns
			2.7V ≤ VDD ≤ 4.4V	41.67	-	ns
			2.4V ≤ VDD ≤ 4.4V	65	-	ns
			1.8V ≤ VDD ≤ 4.4V	125	-	ns
SCLKp high/low voltage level width	tKH1, tKL1	4.0V ≤ VDD ≤ 4.4V		tKCY1/2-4	-	ns
		2.7V ≤ VDD ≤ 4.4V		tKCY1/2-5	-	ns
		2.4V ≤ VDD ≤ 4.4V		tKCY1/2-10	-	ns
		1.8V ≤ VDD ≤ 4.4V		tKCY1/2-19	-	ns
SDIp preparation time (related to SCLKp↑)	tSIK1	4.0V ≤ VDD ≤ 4.4V		12	-	ns
		2.7V ≤ VDD ≤ 4.4V		17	-	ns
		2.4V ≤ VDD ≤ 4.4V		20	-	ns
		1.8V ≤ VDD ≤ 4.4V		28	-	ns
SDIp hold time (related to SCLKp↑)	tKSI1	1.8V ≤ VDD ≤ 4.4V		5	-	ns
SCLKp↓→SDOp Output delay time	tKSO1	1.8V ≤ VDD ≤ 4.4V C=20pF note1		-	5	ns

Note1.:C is the load capacitance of the SCLKp and SDOp output lines.

Attention: Through the port inputmode register and the port outputmode register, the SDIp pin is selected as the normal input buffer and theSDOp pin and SCLKp pin selected as normal output mode.

3) Three-wire SPI mode (slave mode, external clock input)

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, V_{SS}=0V)

Item	Symbol	Condition		-40 ～ +85℃		Unit
				Min	Max	
SCLKp cycle time	tKCY2	4.0V ≤ VDD ≤ 4.4V	20MHz < f_{MCK}	8/f_{MCK}	-	ns
			f_{MCK} ≤20MHz	6/f_{MCK}	-	ns
		2.7V ≤ VDD ≤ 4.4V	16MHz < f_{MCK}	8/f_{MCK}	-	ns
			f_{MCK} ≤16MHz	6/f_{MCK}	-	ns
		2.4V ≤ VDD ≤ 4.4V		6/f_{MCK} and 500	-	ns
		1.8V ≤ VDD ≤ 4.4V		6/f_{MCK} and 750	-	ns
SCLKp high/low level width	tKH2, tKL2	4.0V ≤ VDD ≤ 4.4V		tKCY1/2-7	-	ns
		2.7V ≤ VDD ≤ 4.4V		tKCY1/2-8	-	ns
		1.8V ≤ VDD ≤ 4.4V		tKCY1/2-18	-	ns
SDIp preparation time (To SCLKp↑)	tSIK2	2.7V ≤ VDD ≤ 4.4V		1/f_{MCK}+20	-	ns
		1.8V ≤ VDD ≤ 4.4V		1/f_{MCK}+30	-	ns
SDIp hold time (To SCLKp↑)	tKSI2	1.8V ≤ VDD ≤ 4.4V		1/f_{MCK}+31	-	ns
SCLKp↓→SDOp output delay time	tKSO2	2.7V ≤ VDD ≤ 4.4V C=30pF note1		-	2/f_{MCK}+44	ns
		2.4V ≤ VDD ≤ 4.4V C=30pF note1		-	2/f_{MCK}+75	ns
		1.8V ≤ VDD ≤ 4.4V C=30pF note1		-	2/f_{MCK}+100	ns

Note1: C is the load capacitance of the SCLKp and SDOp output lines.

Attention: Through the port inputmode register and the port outputmode register, select the SDIp pin and SCLKp pin as the normal input buffer and select the SDOp pin as the normal output mode.

4) Four-wire SPI mode (slave mode, external clock input)

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, V_{SS}=0V)

Item	Symbol	Condition		-40 ～ +85℃		Unit
				Min	Max	
SSI00 setup time	tSSIK	DAPmn=0	2.7V ≤ VDD ≤ 4.4V	120	-	ns
			1.8V ≤ VDD ≤ 4.4V	200	-	ns
		DAPmn=1	2.7V ≤ VDD ≤ 4.4V	1/f_{MCK}+120	-	ns
			1.8V ≤ VDD ≤ 4.4V	1/f_{MCK}+200	-	ns
SSI00 hold time	tKSSI	DAPmn=0	2.7V ≤ VDD ≤ 4.4V	1/f_{MCK}+120	-	ns
			1.8V ≤ VDD ≤ 4.4V	1/f_{MCK}+200	-	ns
		DAPmn=1	2.7V ≤ VDD ≤ 4.4V	120	-	ns
			1.8V ≤ VDD ≤ 4.4V	200	-	ns

Note: Through the port input mode register and the port output mode register, select the SDIp pin and SCLKp pin as the normal input buffer and select the SDOp pin as the normal output mode.

5) Simple IIC mode

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, V_{SS}=0V)

Item	Symbol	Condition	-40 ～ +85℃		Unit
			Min	Max	
SCLr Clock frequency	fSCL	2.7V ≤ VDD ≤ 4.4V (Cb = 50 pF, Rb = 2.7 kΩ)	-	1000note1	KHz
		1.8V ≤ VDD ≤ 4.4V (Cb = 100 pF, Rb = 3 kΩ)	-	400note1	KHz
		1.8V ≤ VDD ≤ 2.7V (Cb = 100 pF, Rb = 5 kΩ)	-	300note1	KHz
Hold time when SCLr is low	tLOW	2.7V ≤ VDD ≤ 4.4V (Cb = 50 pF, Rb = 2.7 kΩ)	475	-	ns
		1.8V ≤ VDD ≤ 4.4V (Cb = 100 pF, Rb = 3 kΩ)	1150	-	ns
		1.8V ≤ VDD ≤ 2.7V (Cb = 100 pF, Rb = 5 kΩ)	1550	-	ns
Hold time when SCLr is high	tHIGH	2.7V ≤ VDD ≤ 4.4V (Cb = 50 pF, Rb = 2.7 kΩ)	475	-	ns
		1.8V ≤ VDD ≤ 4.4V (Cb = 100 pF, Rb = 3 kΩ)	1150	-	ns
		1.8V ≤ VDD ≤ 2.7V (Cb = 100 pF, Rb = 5 kΩ)	1550	-	ns
Data setup time(receive)	tSU:DAT	2.7V ≤ VDD ≤ 4.4V (Cb = 50 pF, Rb = 2.7 kΩ)	$1/f_{MCK}$+85note2	-	ns
		1.8V ≤ VDD ≤ 4.4V (Cb = 100 pF, Rb = 3 kΩ)	$1/f_{MCK}$+145note2	-	ns
		1.8V ≤ VDD ≤ 2.7V (Cb = 100 pF, Rb = 5 kΩ)	$1/f_{MCK}$+230note2	-	ns
Data hold time(send)	tHD:DAT	2.7V ≤ VDD ≤ 4.4V (Cb = 50 pF, Rb = 2.7 kΩ)	-	305	ns
		1.8V ≤ VDD ≤ 4.4V (Cb = 100 pF, Rb = 3 kΩ)	-	355	ns
		1.8V ≤ VDD ≤ 2.7V (Cb = 100 pF, Rb = 5 kΩ)	-	405	ns

Note: 1. Must be set to at least fMCK/4.

2. The set value of fMCKcannot exceed the holding time of SCLr="L" and SCLr="H".

7.7.2 Serial Interface IICA

1) I2C standard mode

(TA=-40～+85℃, 1.8V≤VDD≤4.4V, VSS=0V)

Item	Symbol	Condition	Specification Value		Unit
			Min	Max	
SCLA0 Clock frequency	fSCL	Standard mode: f_{CLK}≥1MHz	-	100	KHz
Start condition setup time	tSU: STA	-	4.7	-	μs
Start condition hold time note1	tHD: STA	-	4.0	-	μs
Hold time when SCLA0 is low	tLOW	-	4.7	-	μs
Hold time when SCLA0 is high	tHIGH	-	4.0	-	μs
Data setup time(receive)	tSU:DAT	-	250	-	ns
Data hold time(send)note2	tHD:DAT	-	0	3.45	μs
Stop condition setup time	tSU:STO	-	4.0	-	μs
Bus idle time	tBUF	-	4.7	-	μs

Note:

1) Generate the first clock pulse after generating the start condition or restarting the condition.
2) During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK).

Note: The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Standard mode: Cb=400pF, Rb=2.7kΩ

2) I2C fast mode

(TA=-40～+85℃, 1.8V≤VDD≤4.4V, VSS=0V)

Item	Symbol	Condition	Specification Value		Unit
			Min	Max	
SCLA0 Clock frequency	fSCL	Fast mode: f_{CLK}≥3.5MHz	-	400	KHz
Start condition setup time	tSU: STA	-	0.6	-	μs
Start condition hold time note1	tHD: STA	-	0.6	-	μs
Hold time when SCLA0 is low	tLOW	-	1.3	-	μs
Hold time when SCLA0 is high	tHIGH	-	0.6	-	μs
Data setup time(receive)	tSU:DAT	-	100	-	ns
Data hold time(send)note2	tHD:DAT	-	0	0.9	μs
Stop condition setup time	tSU: STO	-	0.6	-	μs
Bus idle time	tBUF	-	1.3	-	μs

Note:

1) Generate the first clock pulse after generating the start condition or restarting the condition.
2) During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is

necessary to wait for an acknowledgement (ACK).

Note: The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Fast mode: Cb=320pF, Rb=1.1KΩ

3) I2C enhanced fast mode

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, V_{SS}=0V)

Item	Symbol	Condition	Specification Value		Unit
			Min	Max	
SCLA0 Clock frequency	fSCL	Enhanced fast mode: f_{CLK}≥10MHz	-	1000	KHz
Start condition setup time	tSU: STA	-	0.26	-	μs
Start condition hold time note1	tHD: STA	-	0.26	-	μs
Hold time when SCLA0 is low	tLOW	-	0.5	-	μs
Hold time when SCLA0 is high	tHIGH	-	0.26	-	μs
Data setup time(receive)	tSU:DAT	-	50	-	ns
Data hold time(send)note2	tHD:DAT	-	0	0.45	μs
Stop condition setup time	tSU: STO	-	0.26	-	μs
Bus idle time	tBUF	-	0.5	-	μs

Note:

1) Generate the first clock pulse after generating the start condition or restarting the condition.
2) During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK).

Note: The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Enhanced fast mode: Cb=120pF, Rb=1.1KΩ

7.7.3 USB Module Characteristics

1) USB Characteristics

(VCC = VCC_USB = 3.0 to 3.6 V, Ta = -20 to +85°C (USBCLKSEL = 1),
Ta = -40 to +85°C (USBCLKSEL = 0))

Item			Symbol	Specification Value		Unit	Condition
				Min	Max		
Input characteristics	Input high level		VIH	2.0	-	V	-
	Input low level		VIL	-	0.8	V	-
	Differential input sensitivity		VDI	0.2	-	V	DP - DM
	Differential common mode range		VCM	0.8	2.5	V	-
Output characteristics	Output high level		VOH	2.8	VCC_USB	V	-
	Output low level		VOL	0.0	0.3	V	-
	Cross voltage		VCRS	-	-	V	-
	Rising Time	FS	tr	-	-	ns	-
		LS		-	-		
	Falling Time	FS	tf	-	-	ns	-
		LS		-	-		
	Rising & falling time ratio	FS	tr/tf	-	-	%	-
		LS		-	-		
	Output resistance		ZDRV	-	-	Ω	-
VBUS	VBUS Input Voltage		VIH	VCC x 0.8	-	V	-
			VIL	-	VCC x 0.2	V	-
Pull up, pull down	Pull up resistor		RPD	-	-	Ω	-
	Pull-down resistor		RPUI	-	-	Ω	-
			RPUA	-	-	Ω	-
Battery Charging Specifications	D+ leakage current		IDP_SINK	-	-	μA	-
	D- leakage current		IDM_SINK	-	-	μA	-
	DCD source current		IDP_SRC	-	-	μA	-
	Data detection Voltage		VDAT_REF	0.25	0.4	V	-
	D+source Voltage		VDP_SRC	0.5	0.7	V	-
	D-source Voltage		VDM_SRC	0.5	0.7	V	-

2) USB external power supply

Item	Specification Value			Unit	Condition
	Min	Typ	Max		
UVDD Supply current	-	-	50	mA	-
UVDD Supply Voltage	3.0	-	3.6	V	-

7.8 Analog Characteristics

7.8.1 A/D Convertor Characteristics

The distinction of A/D converter characteristics.

Reference Voltage / Input channel	Reference Voltage(+) =AV_{REFP} Reference Voltage (-) =AV_{REFM}	Reference Voltage (+) =V_{DD} Reference Voltage (-) =V_{SS}
ANI0～ANI34	Refer to 7.8.1 1).	Refer to 2).
Internal reference voltage, output voltage of temperature sensor		

1) The scenario while Selecting Reference Voltage (+) =AV_{REFP}/ANI0, Reference Voltage (-)=AV_{REFM}/ANI1:
(TA=-40～+85℃, 1.8V≤AVREFP≤VDD≤4.4V, VSS=0V, Reference Voltage (+)=AVREFP,
Reference Voltage (-)=AVREFM=0V)

Item	Symbol	Condition		Min	Typ	Max	Unit
Resolution	RES	-		-	12	-	bit
Composite error note1	AINL	12 Bit resolution	1.8V ≤AV_{REFP} ≤4.4V	-	3	-	LSB
Conversion time note3	t_{CONV}	12 Bit resolution Conversion Target:ANI2～ANI15	1.8V≤VDD≤4.4V	45	-	-	Tmclk
		12 Bit resolution Conversion Target:Internal Reference Voltage , temperature sensor Output Voltage , PGAOutput Voltage	1.8V≤VDD≤4.4V	72	-	-	Tmclk
Zero scale error note1	E_{ZS}	12 Bit resolution	1.8V ≤AV_{REFP} ≤4.4V	-	0	-	LSB
Full scale error note1	E_{FS}	12 Bit resolution	1.8V ≤AV_{REFP} ≤4.4V	-	0	-	LSB
Integral linearity error note1	ILE	12 Bit resolution	1.8V ≤AV_{REFP} ≤4.4V	-	-	±1	LSB
Differential linearity error note1	DLE	12 Bit resolution	1.8V ≤AV_{REFP} ≤4.4V	-	-	±1.5	LSB
Analog Input Voltage	V_{AIN}	ANI2～ANI34		0	-	AV_{REFP}	V
		Internal Reference Voltage (1.8V≤VDD≤4.4V)		V_{BGR} note2			V
		Temperature sensor Output Voltage (1.8V≤VDD≤4.4V)		V_{TMPS25} note2			V

Note:

1) Does not include quantization error (±1/2 LSB).
2) Please refer to "7.8.5 Characteristics of Temperature Sensor/Internal Reference Voltage".
3) Tmclk is the AD action clock cycle, the maximum action frequency is 64MHz.

2) The scenario while Selecting Reference Voltage(+) =V_{DD}, Reference Voltage (-)=V_{SS}.

(T_A=-40～+85℃, 1.8V≤V_{DD}≤4.4V, V_{SS}=0V, Reference Voltage (+)=V_{DD}, Reference Voltage (-)=V_{SS})

Item	Symbol	Condition		Min.	Typ	Max	Unit
Resolution	RES	-		-	12	-	bit
Composite error note1	AINL	12-bit resolution	1.8V ≤AV_{REFP} ≤4.4V	-	6	-	LSB
Conversion time note3	t_{CONV}	12-bit resolution Conversion target: ANI0～ANI36	1.8V≤VDD≤4.4V	45	-	-	Tmclk
		12-bit resolution Conversion object: internal reference voltage, temperature sensor output voltage, PGA output voltage	1.8V≤VDD≤4.4V	72	-	-	Tmclk
Zero scale error note1	E_{ZS}	12-bit resolution	1.8V ≤AV_{REFP} ≤4.4V	-	0	-	LSB
Full scale error note1	E_{FS}	12-bit resolution	1.8V ≤AV_{REFP} ≤4.4V	-	0	-	LSB
Integral linearity error note1	ILE	12-bit resolution	1.8V ≤AV_{REFP} ≤4.4V	-	-	±2	LSB
Differential linearity error note1	DLE	12-bit resolution	1.8V ≤AV_{REFP} ≤4.4V	-	-	±3	LSB
Analog Input Voltage	V_{AIN}	ANI0～ANI34		0	-	V_{DD}	V
		internal Reference Voltage (1.8V≤VDD≤4.4V)		V_{BGR} note2			V
		Temperature sensor Output Voltage (1.8V≤VDD≤4.4V)		V_{TMPS25} note2			V

Note:

1) Does not include quantization error (±1/2 LSB).

2) Please refer to "7.8.5 Characteristics of Temperature Sensor/Internal Reference Voltage".

3) Tmclk is the AD action clock cycle, the maximum action frequency is 64MHz.

7.8.2 Sigma-Delta ADC Maximum Rating

Name	Symbol	Min	Max	Unit
Power supply Voltage	AVDD	-0.3	4.4	V
Digitla pin Input Voltage	-	-0.3	AVDD+0.3	V
Operating temperature	-	-40	85	℃

7.8.3 Sigma-Delta ADC Digital Logic Characteristics

Parameter	Min	Typ	Max	Unit	Condition
VIH	0.7xAVDD	-	AVDD+0.1	V	-
VIL	AGND	-	0.3xAVDD	V	-
VOH	AVDD-0.4	-	AVDD	V	-
VOL	AGND	-	0.2xAVDD	V	-
serial Clock SCLK operating frequency	0.1	-	1.1	MHz	-

7.8.4 Sigma-Delta ADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Analog Input					
Full scale differential Input Voltage	-REFIN/PGA	-	REFIN/PGA	V	-
Common mode Input Voltage	GND+0.75	-	VDD-1	V	-
Differential Input impedance	-	250	-	Mohm	-
System performance					
Resolution	-	24	-	bits	No missing code data
Output rate	2.5	5	2.56K	Hz	-
Setup time	-	-	3	conversion cycle	full build
Equivalent Input noise	-	30	-	nVrms	PGA=128, 10Hz, LDO=3V
Effective resolution	-	20.6	-	bits	PGA=128, 10Hz, LDO=3V
Offset error	-	2.5	10	uV	PGA=64,128
Offset error drifting	-	30	-	nV/℃	PGA=64,128
Gain Error	-	±1.5	-	%	PGA=64,128
Gain Error drifting	-	16	-	ppm/℃	PGA=64,128
Reference Voltage Input	0.5	LDOOUT	LDOOUT	V	-
Temperature sensing	-	±3	-	℃	-
Bandgap Reference Voltage	-	1.24	-	V	VDD=3.3V
LDO Electrical characteristics					
Output Voltage	-	3.07	-	V	SET_LDO[1:0]=00
	-	2.66	-	V	SET_LDO[1:0]=10
Loading capacity	-	20	-	mA	VDD=3.3V
Power supply Electrical characteristics					
Power Supply Voltage	2.5	3.3	4.4	V	-
Normal operation current	-	1.68	-	mA	PGA=128
	-	0.83	-	mA	PGA=2
Sleep mode current	-	50	-	nA	-

Below Table shows different output rate, effective resolutions under different PGA gain condition of the Sigma-Delta ADC. Test condition: Power supply voltage 3.3V, temperature 27 Degree, LDO configured to be 3V Output, reference voltage as LDO Output Voltage, Input common mode Voltage is 0.5 times LDO Output Voltage, Input differential Voltage as 0V, Single Chip under each configuration has total data size of 1000.

Effective Resolution=Log2 (2*REFIN /RMS_Noise)

Effective Resolution	FADC	656K (FADC=1)							
	OSR	64	128	256	1024	4096	8192	16384	32768
	ODR (Hz)	2560	1280	640	160	40.0	20.0	10	5
PGA Gain	2 (0000b)	15.0	17.4	18.6	19.8	20.7	21.2	21.7	22.1
	4 (0001b)	15.0	17.2	18.5	19.6	20.5	21.2	21.7	22.1
	8 (0011b)	14.9	17.3	18.4	19.5	20.5	21.0	21.6	22.1
	16 (0100b)	15.1	17.3	18.4	19.5	20.5	21.2	21.6	22.1
	32 (0101b)	15.0	17.1	18.2	19.3	20.3	20.8	21.4	21.8
	64 (0110b)	15.1	17.2	18.1	19.3	20.3	20.8	21.3	21.8
	128 (0111b)	14.9	16.7	17.6	18.7	19.7	20.1	20.6	21.1
	256 (1000b)	14.8	16.0	16.7	17.8	18.8	19.2	19.8	20.3

7.8.5 Characteristics of Temperature Sensor/internal Reference Voltage

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, VSS=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
The output voltage of the temperature sensor	VTMPS25	ADS Register=80H, TA=+25℃	-	1.09	-	V
Internal reference voltage	VBGR	ADS Register=81H	1.38note	1.45	1.5note	V
Temperature Coefficient	FVTMPS	-	-	-3.5	-	mV/℃
Stable operation waiting time	tAMP	-	5	-	-	μs

Note:1. Low temperature Specification Value is guaranteed by design, mass production does not measure low temperature conditions.

7.8.6 Comparator

(T_A=-40～+85℃, 1.8V≤VDD≤4.4V, V_{SS}=0V)

item	symbol	condition		MIN	TYP	MAX	unit
Input deviation Voltage	V_{IOCMP}	-		-	±10	±40	mV
Input Voltage range	Ivcmp	-		0	-	VDD	V
Internal Reference Voltage deviation	ΔV_{IREF}	CmRVM register:7FH ~ 80H (m = 0, 1)		-	-	±2	LSB
		Others		-	-	±1	LSB
Response time	tCR, tCF	Input amplitude±100mV		-	70	150	ns
Stable operation timenote1	tCMP	CMPn=0->1	VDD= 3.3 ~ 4.4V	-	-	1	μs
			VDD= 1.8 ~ 3.3V	-	-	3	
Reference Voltage stabilization time	tVR	CVRE=0->1 note2		-	-	20	μs
operating current	I_{CMPDD}	it is defined as the operation current of peripheral functions					-

Note1: The time required from the enable of the comparator action (CMPnEN=0 —>1) to meeting the various DC/AC style requirements of CMP.

Note2: After the internal reference voltage generator is enabled (by setting the CVREm bit to 1; m = 0 to 1), the comparator output can be enabled after the reference voltage stabilization time (CnOE bit = 1; n = 0 to 1).

7.8.7 PGA Electrical Characteristic

T_A＝25℃, VDD＝4.4V, V_{IN+}=0.01V, unless otherwise specified. (G is the gain multipler)

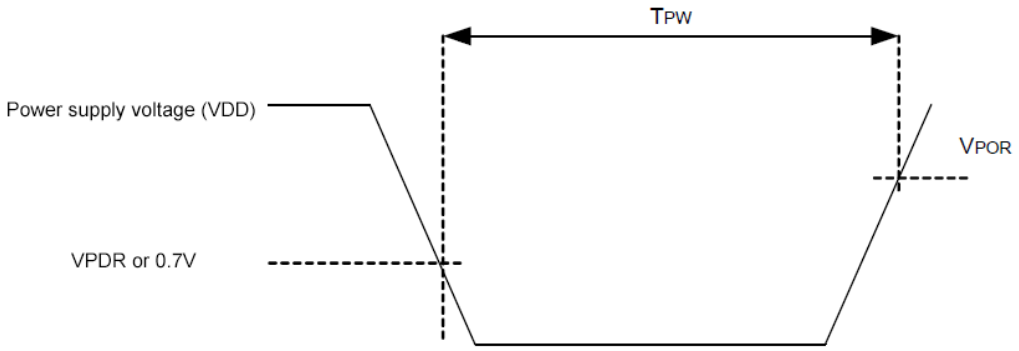
Symbol	Parameter	Condition	Min value	Typical value	Max value	Unit
VDD	Power supply Voltage	-	2.5	-	4.4	V
I_Q	Quiescent Current	V_{OUT}=2V	-	0.5	0.7	mA
I_{SD}	Shutdown current	-	-	10	-	nA
T_A	Operating temperature	-	-40	25	85	℃
Input characteristics						
V_{OS}	Input offset Voltage	Not calibrated (PGAADJ=20H)	-	±2.5	-	mV
		After Calibration	-	±0.1	±0.2	
V_{CM}	Common Mode Input Voltage Range	G=1	0.032	-	(VDD-1.5)/ G	V
		G=2	0.016			
		G=4	0.008			
		G=8	0.004			
		G=16	0.002			
		G=32, 64,128	0.001			
I_B	Input bias current	-	-	10	-	pA
I_{OS}	Input offset current	-	-	10	-	pA
Output characteristics						
EG	Gain Error	G=1, 2, 4, 8, 16	-1	-	1	%
		G=32	-2	-	2	
		G=64,128	-4	-	4	
C_{LOAD}	Capacitive load	-	-	10	-	pF
V_{OH}	Maximum Output Voltage	-40℃~85℃	-	-	VDD-1.5	V
V_{OL}	Minimum Output Voltage	-40℃~85℃	0.032	-	-	V
Frequency characteristics						
BW	bandwidth	C_{LOAD}=10pF,G=1	-	1.5	-	MHz
PSRR	Power supply rejection ratio	VDD=2.5~4.4V,G=16	-	75	-	dB
CMRR	Common mode rejection ratio	-40℃~85℃	-	80	-	dB
Transient characteristics						
SR	Slew rate	C_{LOAD}=10pF,G=32	-	10	-	V/μs
T_{STB}	Stablization Time	-	-	-	2	μs
$T_{SH(1)}$	Sampling Hold Time	-	-	3	-	μs

7.8.8 POR Circuit Characteristics

(T_A=-40～+85℃, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Detection Voltage	VPOR	Power supply Voltage Rising		1.60	1.75	V
	VPDR	Power supply Voltage Falling	1.37	1.50	1.55	V
Minimum Pulse Width note1	TPW	-	300	-	-	μs

Note1: This is the time required for POR to reset when VDD is lower than VPDR. In addition, in the deep sleep mode, when the main system clock (fMAIN) is stopped by setting bit0 (HIOSTOP) and bit7 (MSTOP) of the clock operation status control register (CSC), the oscillation of the main system clock (fMAIN) is stopped, it is the time required for POR reset from VDD lower than 0.7V to rise above VPOR.



7.8.9 LVD Circuit Characteristics

1) Reset mode and interrupt mode

(T_A=-40～+85℃, $V_{PDR} \leqslant V_{DD} \leqslant$4.4V, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
Detection Voltage	VLVD0	Power Supply Voltage Rising	-	4.06	-	V
		Power Supply Voltage Falling	-	3.98	-	V
	VLVD1	Power Supply Voltage Rising	-	3.75	-	V
		Power Supply Voltage Falling	-	3.67	-	V
	VLVD2	Power Supply Voltage Rising	-	3.13	-	V
		Power Supply Voltage Falling	-	3.06	-	V
	VLVD3	Power Supply Voltage Rising	-	3.02	-	V
		Power Supply Voltage Falling	-	2.96	-	V
	VLVD4	Power Supply Voltage Rising	-	2.92	-	V
		Power Supply Voltage Falling	-	2.86	-	V
	VLVD5	Power Supply Voltage Rising	-	2.81	-	V
		Power Supply Voltage Falling	-	2.75	-	V
	VLVD6	Power Supply Voltage Rising	-	2.71	-	V
		Power Supply Voltage Falling	-	2.65	-	V
	VLVD7	Power Supply Voltage Rising	-	2.61	-	V
		Power Supply Voltage Falling	-	2.55	-	V
	VLVD8	Power Supply Voltage Rising	-	2.50	-	V
		Power Supply Voltage Falling	-	2.45	-	V
	VLVD9	Power Supply Voltage Rising	-	2.09	-	V
		Power Supply Voltage Falling	-	2.04	-	V
	VLVD10	Power Supply Voltage Rising	-	1.98	-	V
		Power Supply Voltage Falling	-	1.94	-	V
	VLVD11	Power Supply Voltage Rising	-	1.88	-	V
		Power Supply Voltage Falling	-	1.84	-	V
Minimum pulse width	tLW	-	300	-	-	μs
Detection delay	-	-	-	-	300	μs

1) Interrupt and reset mode

(T_A=-40～+85℃, V_{PDR} ≤V_{DD}≤4.4V, V_{SS}=0V)

Item	Symbol	Condition			Min	Typ	Max	Unit
interrupt or reset mode	V_{LVDA0}	V_{POC2}，V_{POC1}，V_{POC0}=0，0，0, Falling reset Voltage			-	1.63	-	V
	V_{LVDA1}		LVIS1，LVIS0=1，0	rising reset release voltage	-	1.77	-	V
				Falling interrupt Voltage	-	1.73	-	V
	V_{LVDA2}		LVIS1，LVIS0=0，1	rising reset release voltage	-	1.88	-	V
				Falling interrupt Voltage	-	1.84	-	V
	V_{LVDA3}		LVIS1，LVIS0=0，0	rising reset release voltage	-	2.92	-	V
				Falling interrupt Voltage	-	2.86	-	V
	V_{LVDB0}	V_{POC2}，V_{POC1}，V_{POC0}=0，0，1, Falling reset Voltage			-	1.84	-	V
	V_{LVDB1}		LVIS1，LVIS0=1，0	rising reset release voltage	-	1.98	-	V
				Falling interrupt Voltage	-	1.94	-	V
	V_{LVDB2}		LVIS1，LVIS0=0，1	rising reset release voltage	-	2.09	-	V
				Falling interrupt Voltage	-	2.04	-	V
	V_{LVDB3}		LVIS1，LVIS0=0，0	rising reset release voltage	-	3.13	-	V
				Falling interrupt Voltage	-	3.06	-	V
	V_{LVDC0}	V_{POC2}，V_{POC1}，V_{POC0}=0，1，0, Falling reset Voltage			-	2.45	-	V
	V_{LVDC1}		LVIS1，LVIS0=1，0	rising reset release voltage	-	2.61	-	V
				Falling interrupt Voltage	-	2.55	-	V
	V_{LVDC2}		LVIS1，LVIS0=0，1	rising reset release voltage	-	2.71	-	V
				Falling interrupt Voltage	-	2.65	-	V
	V_{LVDC3}		LVIS1，LVIS0=0，0	rising reset release voltage	-	3.75	-	V
				Falling interrupt Voltage	-	3.67	-	V
	V_{LVDD0}	V_{POC2}，V_{POC1}，V_{POC0}=0，1，1, Falling reset Voltage			-	2.75	-	V
	V_{LVDD1}		LVIS1，LVIS0=1，0	rising reset release voltage	-	2.92	-	V
				Falling interrupt Voltage	-	2.86	-	V
	V_{LVDD2}		LVIS1，LVIS0=0，1	rising reset release voltage	-	3.02	-	V
				Falling interrupt Voltage	-	2.96	-	V
	V_{LVDD3}		LVIS1，LVIS0=0，0	rising reset release voltage	-	4.06	-	V
				Falling interrupt Voltage	-	3.98	-	V

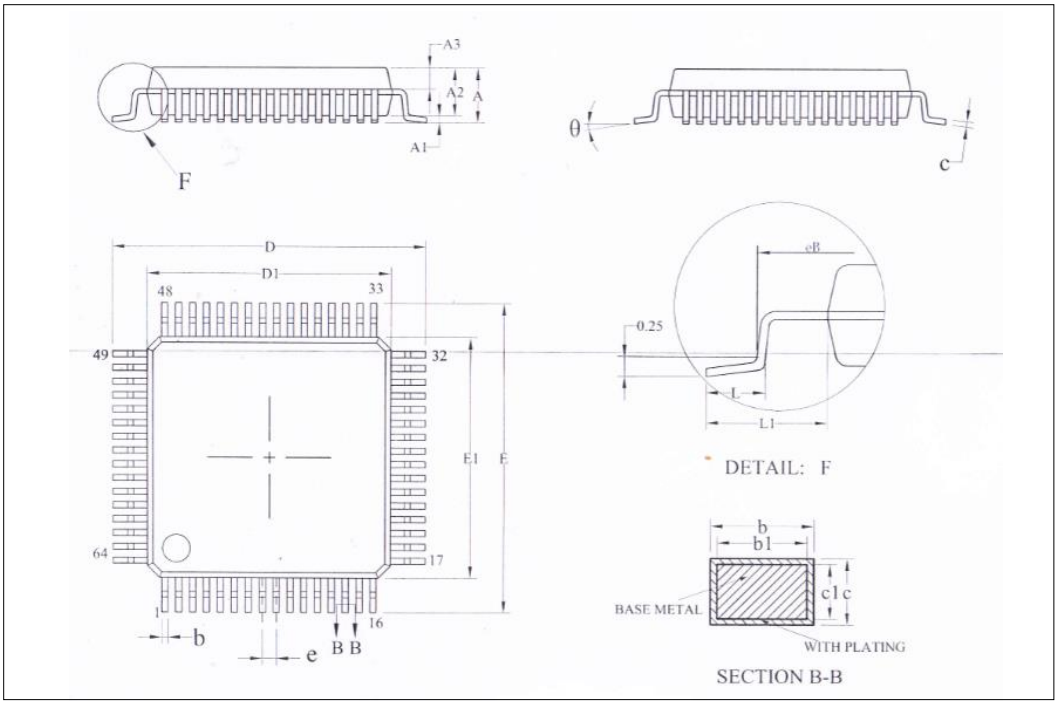
7.8.10 The Rising Slope of The Power Supply Voltage Characteristic

(T_A=-40～+85℃, V_{SS}=0V)

Item	Symbol	Condition	Min	Typ	Max	Unit
The rising slope of the power supply voltage	SVDD	-	-	-	54	V/ms

8 Package Information

8.1 LQFP64



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.40BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0	-	7°

9 Version History

Version No	Time	Modification Content
V1.00	2021 April	Initial version
V1.01	2021 September	Modified supply Voltage range, Sigma-Delta ADC related error
V1.11	2021 November	Modified Temperature Voltage etc parameters
V1.12	2021 December	Added pin description and deleted unnecessary temperature parameters
V1.13	2022 January	Refined some descriptions