BAT32G135 Datasheet

LowPower-line Arm®-based 32-bit MCU with up to 64KB Flash,

Analog functions, Timers and Communication interfaces.

V1.4.2

Please note the following CMS IP policy

Features

- **Ultra-low power consumption technology**
  - Operating Voltage:1.8V~5.5V
  - Operating ambient temperature: -40℃~105℃
  - Low power modes: SLEEP, DEEPSLEEP
  - Operating power consumption:
    RUN mode: 35uA/MHz@64MHz
    DEEPSLEEP mode:0.45uA
    DEEPSLEEP mode (+32.768K+RTC):0.7uA
- **Core**
  - ARM®32-bitCortex®-M0+ CPU
  - Operating frequency:32KHz~64MHz
- **Memories**
  - 64KB Flash Memory: program/data flash
  - 1.5KB Special data flash memory
  - 8KB SRAM Memory (With Parity)
- **Reset and power management**
  - Power-on reset circuit.
  - On-chip voltage detector (LVD) (Select interrupt and reset level by option byte)
- **Clock**
  - Main clock oscillator: 1MHz to 64MHz
  - Sub clock oscillator: 32.768KHz
  - High-speed on-chip oscillator: 1MHz to 20MHz, accuracy (±1%)
  - Low-speed on-chip oscillator: 15KHz
- **Multiplier**
  - Integer multiplier
- **DMA**
  - Interupt trigger start.
  - Transfer modes: Normal mode, Repeat mode, Block mode and Chain transfers mode
  - Transfer space: 4 GB area from 0000 0000h to FFFF FFFFh except reserved areas
- **EVENTC**
  - Event Link Controller
  - Event signals (15 types) can be used as activation sources for operating any one of 4 types of peripheral functions
- **Analog**
  - 12-Bit A/D Converter
    Conversion range: 0 to Vrefp or VDD
  - Analog input: Up to 15 channels, Internal reference voltage (1.45 V) and temperature sensor
  - Conversionrate: 1.42Msps
  - Comparator (CMP) × 2: The external reference voltage or internal reference voltage can be selected as the reference voltage
  - Programmable gain amplifier (PGA)×2: GAIN x4/8/10/12/14/16/32 can be selected
- **GPIO**
  - I/O port: 29 to 45
  - Can be set to N-ch open drain and on-chip pull-up resistor
  - Digital function can be freely assigned to any pin
  - On-chip clock output/buzzer output controller
- **Serial wire debug (SWD)**
- **Timers**
  - 16-bit timer: 8 channels
  - 15-bit interval timer: 1 channel
  - Real-time clock (RTC): 1 channel
  - Watchdog timer (WWDT): 1 channel (operable with the dedicated low-speed on-chip oscillator)
  - SysTick timer
- **Serial interfaces**
  - SCI: 3 channels (1 UART / 2 SPI / 2 I2C for each SCI channel)
  - Standard SPI:1 channel (8bit or 16bit)
  - Standard I2C:1 channel
  - IrDA:1 channel
- **Safety**
  - IEC/UL 60730
  - Illegal memory access
  - SRAM Parity Error Check
  - Cyclic Redundancy Check (CRC) Calculator
  - SFR protection
  - 128-bit unique ID
  - Flash secondary protection in debug mode (level1: only erase the entire area of flash; level2: the emulator connection is invalid)
- **Packages**
  - 48LQFP, 40QFN, 32LQFP, 32QFN

1 Overview

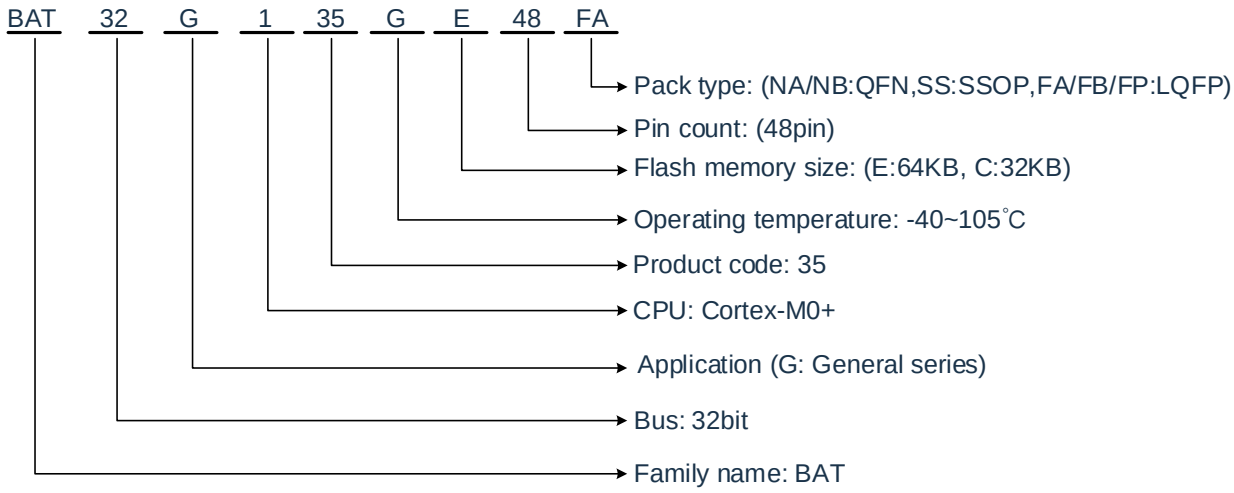
1.1 Introduction

The ultra-low-power BAT32G135 incorporates a high-performance ARM®Cortex®-M0+ 32-bit RISC core running up to 64 MHz and high-speed embedded flash memory (SRAM maximum 8KB, program/data flash 64KB). This product integrates I2C, SPI, UART, LIN multiple standard interfaces. Integrated 12bitA/D converter, temperature sensor, 8bitD/A converter, comparator, programmable gain amplifier. Among them, the 12bitA/D converter can collect external sensor signals to reduce the system design cost. The temperature integrated sensor can realize real-time monitoring of the external ambient temperature. The inner comparator can support high-speed and low-speed operating modes. In high-speed mode, it can support high-speed motor control feedback, and in low-speed mode, it can be used for battery monitoring. Integrated 8-channel 16bit timer module with EPWM control circuit, combined with the timer can realize the control of a DC motor or two stepper motors.

BAT32G135 has particularly excellent low-power performance, with two low-power modes of sleep and deep sleep, to flexible design for users. Its operating power consumption is 35uA/MHz@64MHz, and the power consumption in deep sleep mode is only 0.45uA, which is suitable for battery-powered low-power devices. At the same time, due to the integrated event link controller, direct connection between hardware modules can be achieved without CPU intervention, which is faster than the use of interrupt response, while reducing the CPU's activity frequency and extending battery life.

These features make the BAT32G135 microcontroller series widely applicable to energy storage, battery packs, motor control, security, power, and other applications.

1.2 Ordering Information



BAT32G135 Product list:

Pin count	Package	Ordering Part Number
32 pins	32 LQFP（7x7mm，0.8mm pitch）	BAT32G135GE32FP
32 pins	32 QFN（5x5mm，0.5mm pitch）	BAT32G135GE32NA
40 pins	40 QFN（5x5mm，0.4mm pitch）	BAT32G135GE40NB
48 pins	48 LQFP（7x7mm，0.5mm pitch）	BAT32G135GE48FA

FLASH, SRAM:

Flash memory	Special data flash memory	SRAM	32 Pins / 40 Pins / 48 Pins		
64KB	1.5KB	8KB	BAT32G135GE32	BAT32G135GE40	BAT32G135GE48

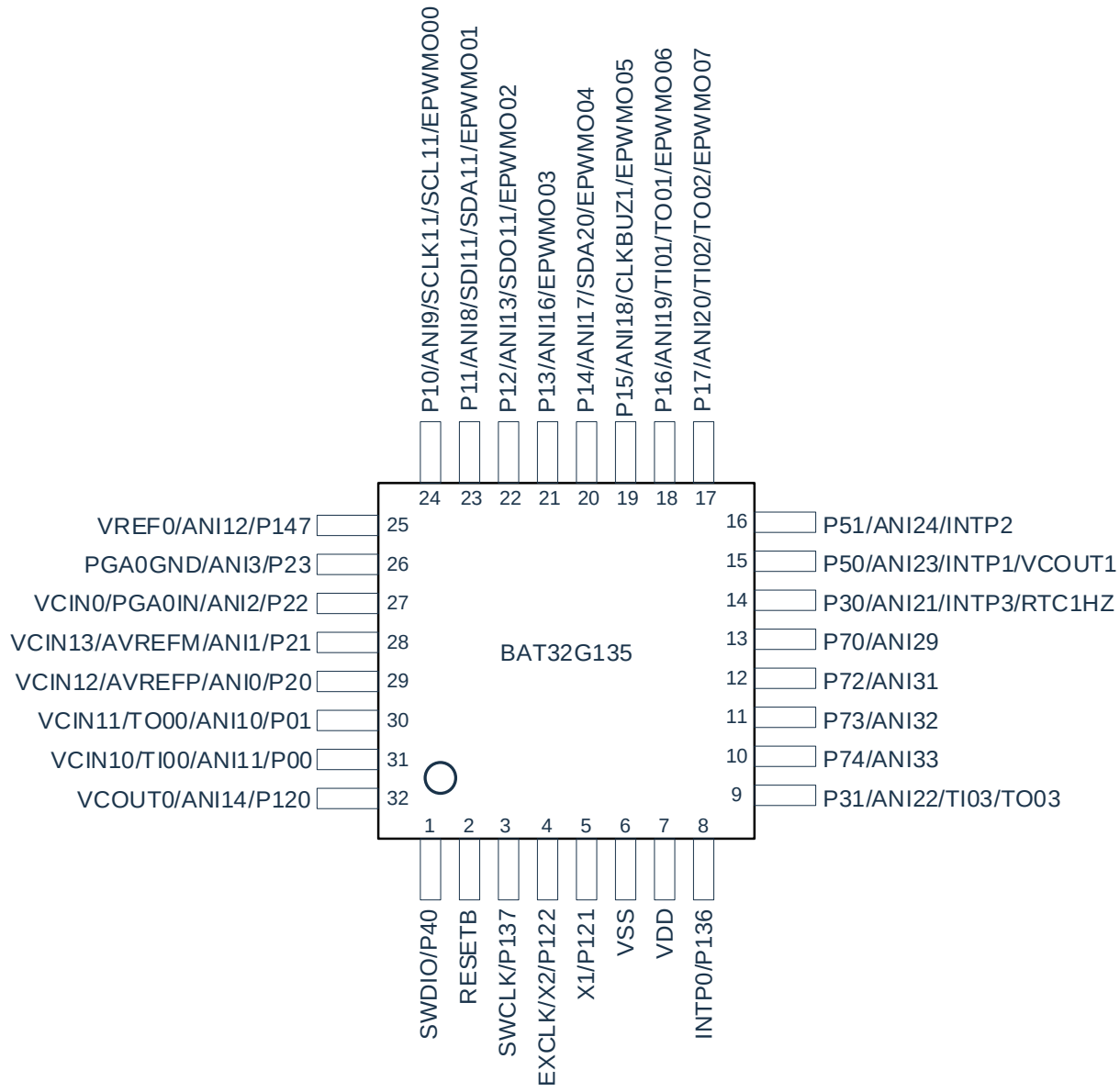
BAT32G135 product selection table:

Part No.	Core	Operating frequency (MHz)	Min. operating voltage (V)	Max. operating voltage (V)	Code Flash (kB)	SRAM (kB)	Data Flash (kB)	DMA	GPIO	12bit ADC	Comparator CMP	Amplifier PGA	Universal timer (16bit)	Real-time clock (RTC)	Watchdog timer (WDT)	Universal asynchronous receiver/transmitter (UART)	Serial peripheral interface (SPI)	IIC bus	IrDA bus	Hardware multiplier	Hardware divider	Package
BAT32G135 GE32FP	M0+	64	1.8	5.5	64	8	1.5	24	29	25+3	2	1	8	1	1	3	1+3	1+3	1	Y	Y	LQFP32
BAT32G135 GE32NA	M0+	64	1.8	5.5	64	8	1.5	24	29	25+4	2	1	8	1	1	3	1+3	1+3	1	Y	Y	QFN32
BAT32G135 GE40NB	M0+	64	1.8	5.5	64	8	1.5	24	37	28+4	2	2	8	1	1	3	1+4	1+4	1	Y	Y	QFN40
BAT32G135 GE48FA	M0+	64	1.8	5.5	64	8	1.5	24	45	35+4	2	2	8	1	1	3	1+5	1+5	1	Y	Y	LQFP48

1.3 Pin Configuration (Top View)

1.3.1 BAT32G135GE32FP

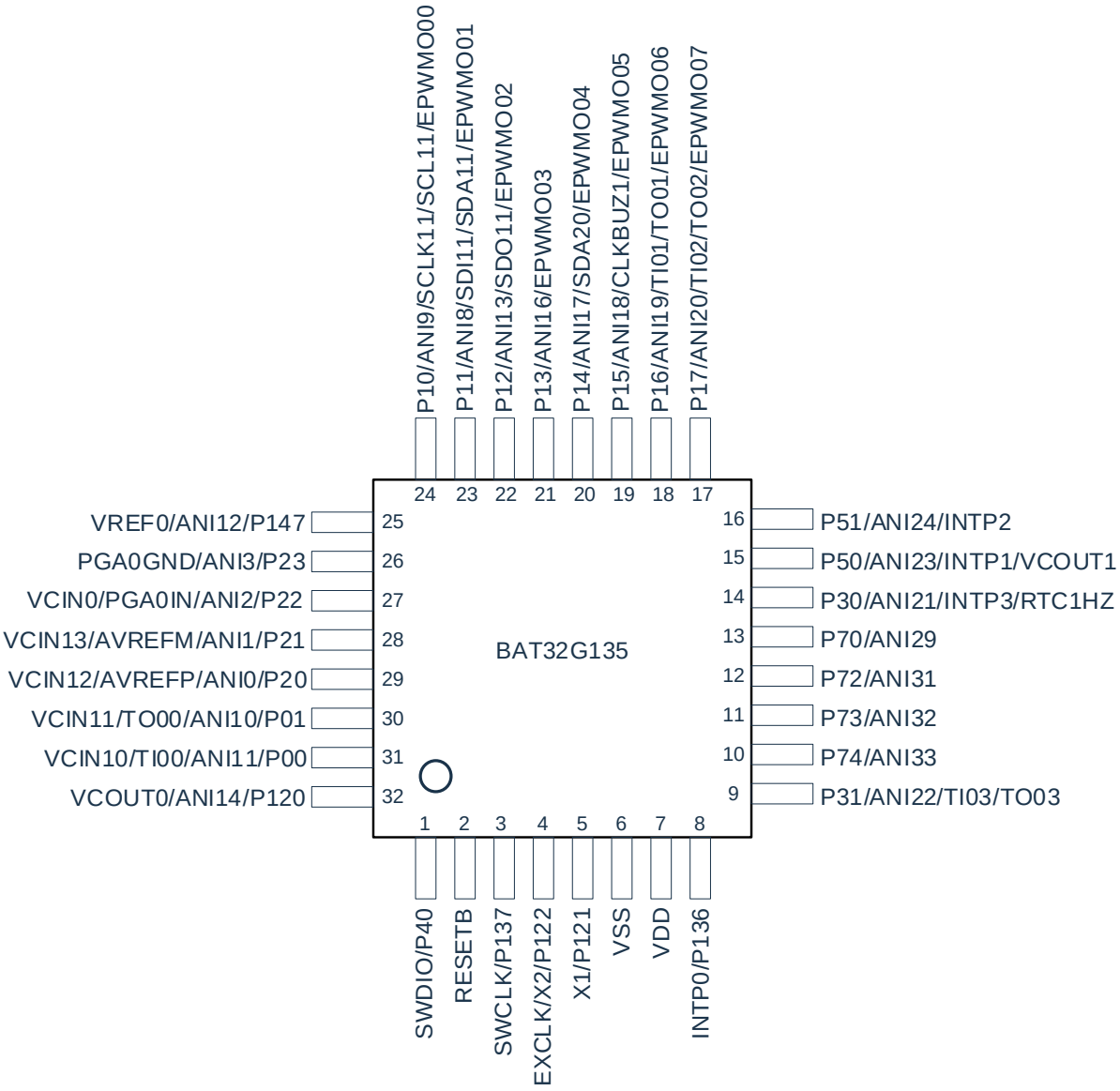
- 32LQFP (7x7mm, 0.8mm pitch)



Remark: Digital function supports pins that are not marked in the figure can be configured. Refer to section 4.1

1.3.2 BAT32G135GE32NA

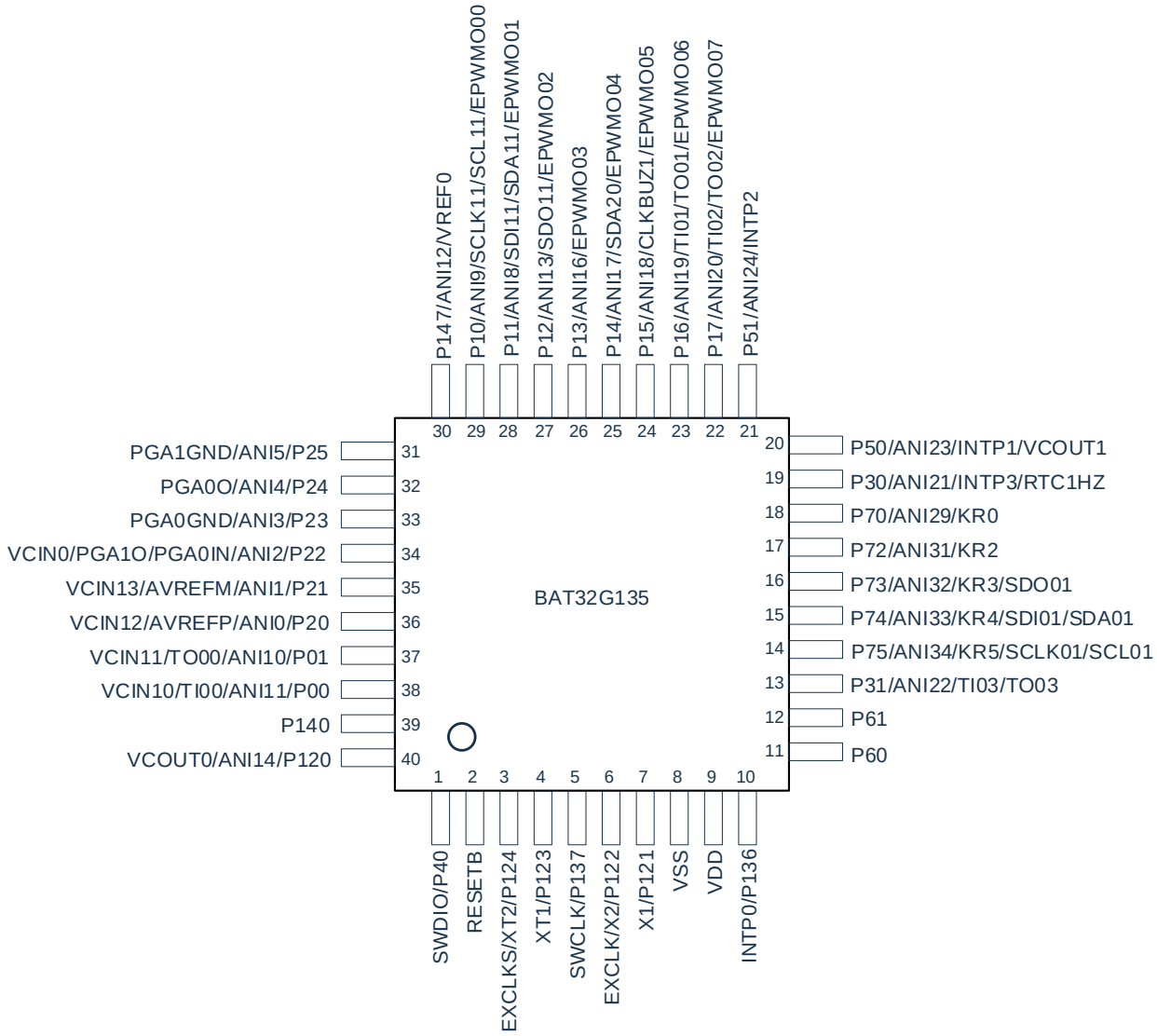
- 32QFN（5x5mm, 0.5mm pitch）



Remark: Digital function supports pins that are not marked in the figure can be configured. Refer to section 4.1

1.3.3 BAT32G135GE40NB

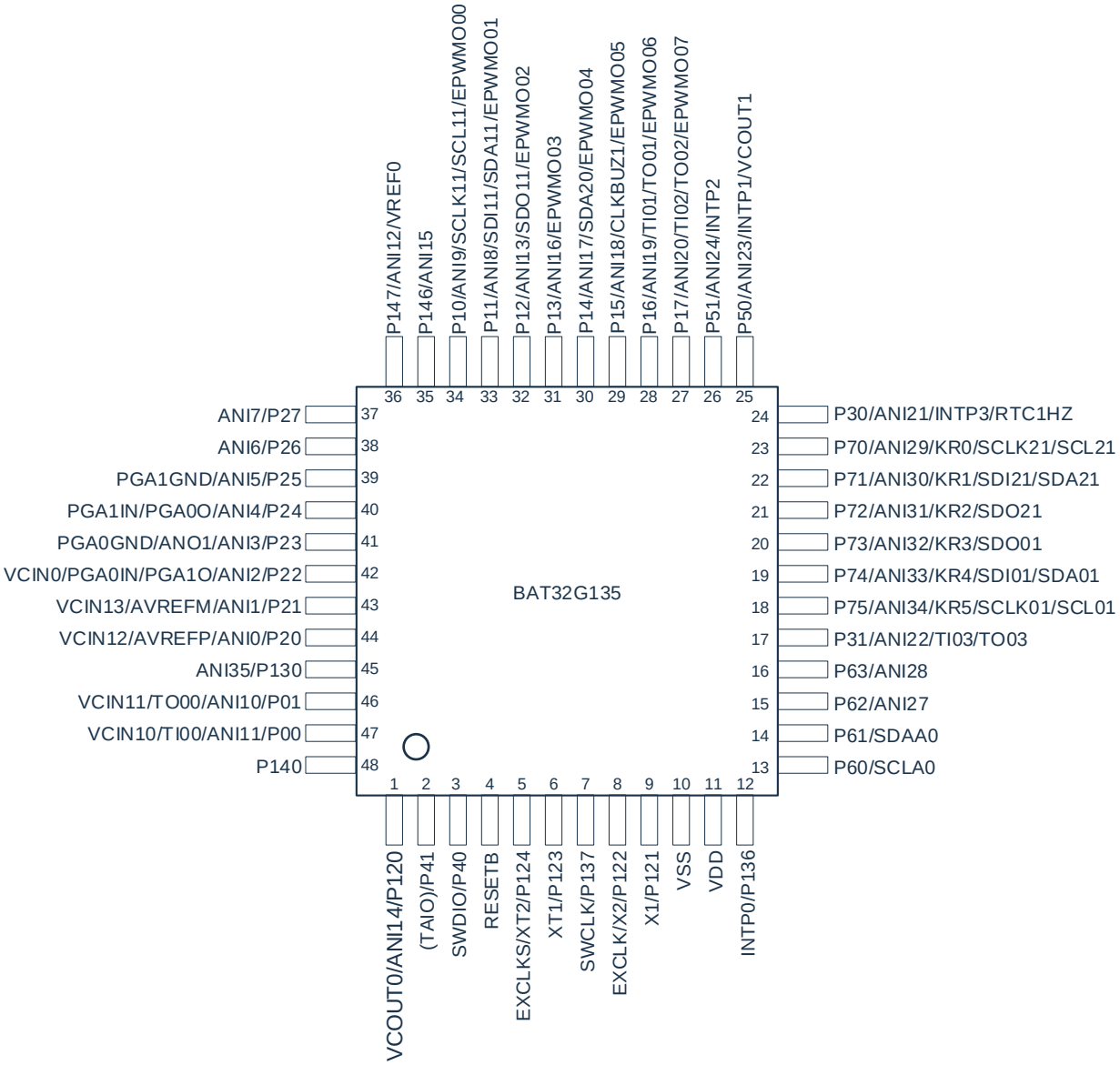
- 40QFN (5x5mm, 0.4mm pitch)



Remark: Digital function supports pins that are not marked in the figure can be configured. Refer to section 4.1

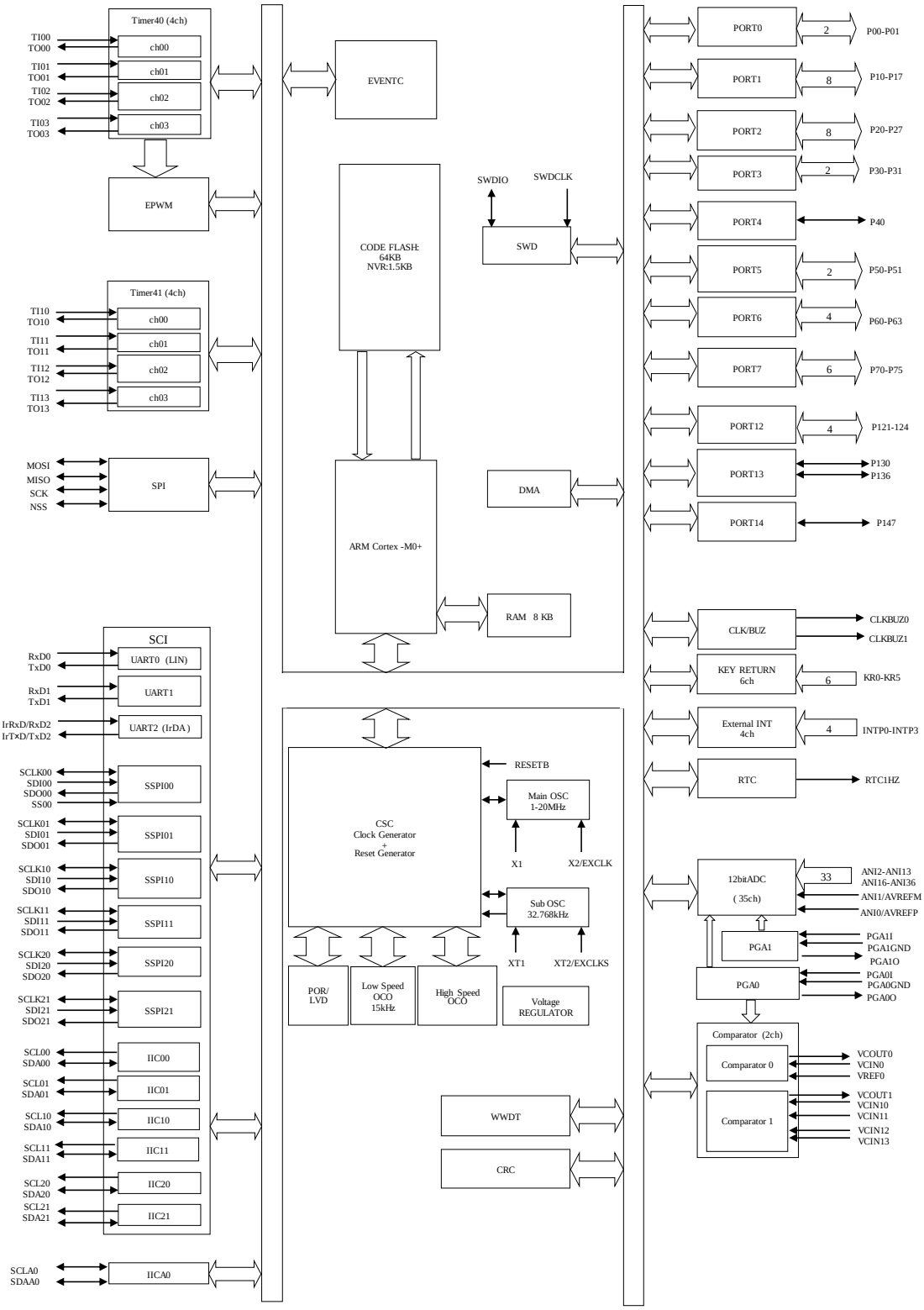
1.3.4 BAT32G135GE48FA

- 48LQFP (7x7mm, 0.5mm pitch)

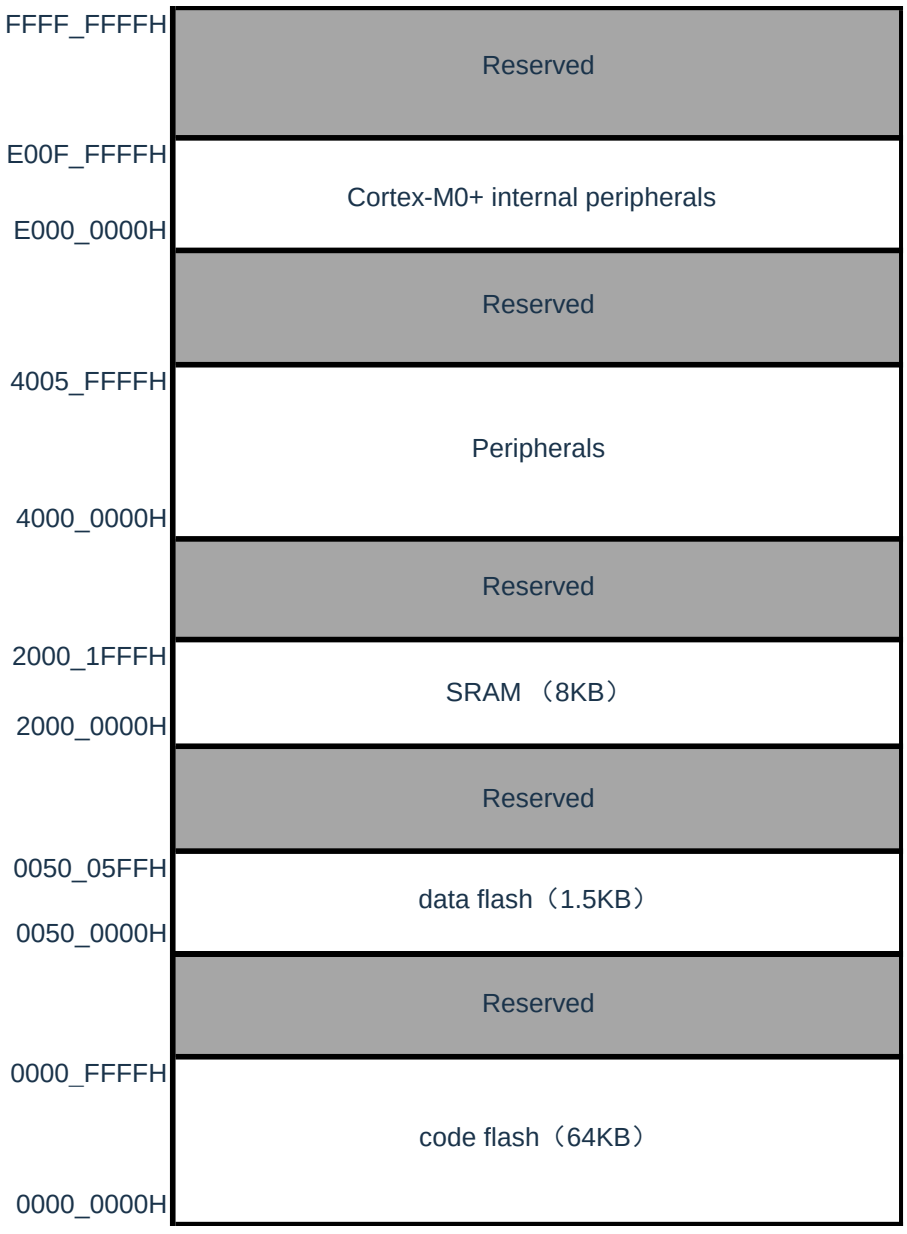


Remark: Digital function supports pins that are not marked in the figure can be configured. Refer to section 4.1

2 Block Diagram



3 Memory Space



4 PIN Funtions

4.1 Port Functions

Table 4.1.1

Port Name	Alternate Function	Digital output function configuration register pxxcfg[3:0]	Digital input function configuration register xxxPCFG[5:0]	Function built-in or not		
				48LQFP	40QFN	32LQFP 32QFN
RESETB	RESETB	-	-	●	●	●
P00	GPIO	00H	00H	●	●	●
	ANI11	00H	00H	●	●	●
	VCIN10	00H	00H	●	●	●
	TI00	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P01	GPIO	00H	00H	●	●	●
	ANI10	00H	00H	●	●	●
	VCIN11	00H	00H	●	●	●
	TO00	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P10	GPIO	00H	00H	●	●	●
	ANI9	00H	00H	●	●	●
	SCLK11	00H	00H	●	●	●
	SCL11	00H	00H	●	●	●
	EPWMO00	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P11	GPIO	00H	00H	●	●	●
	ANI8	00H	00H	●	●	●
	SDI11	00H	00H	●	●	●
	SDA11	00H	00H	●	●	●
	EPWMO01	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P12	GPIO	00H	00H	●	●	●
	ANI13	00H	00H	●	●	●
	SDO11	00H	00H	●	●	●
	EPWMO02	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P13	GPIO	00H	00H	●	●	●
	ANI16	00H	00H	●	●	●
	EPWMO03	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●

P14	GPIO	00H	00H	●	●	●
	ANI17	00H	00H	●	●	●
	SDA20	00H	00H	●	●	●
	EPWMO04	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P15	GPIO	00H	00H	●	●	●
	ANI18	00H	00H	●	●	●
	CLKBUZ1	00H	00H	●	●	●
	EPWMO05	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P16	GPIO	00H	00H	●	●	●
	ANI19	00H	00H	●	●	●
	TI01	00H	00H	●	●	●
	TO01	00H	00H	●	●	●
	(SPIMOSI)	00H	00H	●	●	●
	EPWMO06	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P17	GPIO	00H	00H	●	●	●
	ANI20	00H	00H	●	●	●
	TI02	00H	00H	●	●	●
	TO02	00H	00H	●	●	●
	(SPIMISO)	00H	00H	●	●	●
	EPWMO07	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P20	GPIO	00H	00H	●	●	●
	ANI0	00H	00H	●	●	●
	AVREFP	00H	00H	●	●	●
	VCIN12	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P21	GPIO	00H	00H	●	●	●
	ANI1	00H	00H	●	●	●
	AVREFM	00H	00H	●	●	●
	VCIN13	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P22	GPIO	00H	00H	●	●	●
	ANI2	00H	00H	●	●	●
	PGA0IN	00H	00H	●	●	●
	PGA1O	00H	00H	●	●	-
	VCIN0	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P23	GPIO	00H	00H	●	●	●
	ANI3	00H	00H	●	●	●

	PGA0GND	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P24	GPIO	00H	00H	●	●	-
	ANI4	00H	00H	●	●	-
	PGA1IN	00H	00H	●	●	-
	PGA0O	00H	00H	●	●	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	-
P25	GPIO	00H	00H	●	●	-
	ANI5	00H	00H	●	●	-
	PGA1GND	00H	00H	●	●	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	-
P26	GPIO	00H	00H	●	-	-
	ANI6	00H	00H	●	-	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	-	-
P27	GPIO	00H	00H	●	-	-
	ANI7	00H	00H	●	-	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	-	-
P30	GPIO	00H	00H	●	●	●
	ANI21	00H	00H	●	●	●
	INTP3	00H	00H	●	●	●
	RTC1HZ	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P31	GPIO	00H	00H	●	●	●
	ANI22	00H	00H	●	●	●
	TI03	00H	00H	●	●	●
	TO03	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P40	GPIO	00H	00H	●	●	●
	SWDIO	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P41	GPIO	00H	00H	●	-	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	-	-
P50	GPIO	00H	00H	●	●	●
	ANI23	00H	00H	●	●	●
	INTP1	00H	00H	●	●	●
	VCOUT1	00H	00H	●	●	●
	(SPINSS)	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P51	GPIO	00H	00H	●	●	●
	ANI24	00H	00H	●	●	●
	INTP2	00H	00H	●	●	●
	(SPISCK)	00H	00H	●	●	●

	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P60	GPIO	00H	00H	●	●	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	-
P61	GPIO	00H	00H	●	●	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	-
P62	GPIO	00H	00H	●	-	-
	ANI27	00H	00H	●	-	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	-	-
P63	GPIO	00H	00H	●	-	-
	ANI28	00H	00H	●	-	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	-	-
P70	GPIO	00H	00H	●	●	●
	ANI29	00H	00H	●	●	●
	KR0	00H	00H	●	●	-
	SCLK21	00H	00H	●	-	-
	SCL21	00H	00H	●	-	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P71	GPIO	00H	00H	●	-	-
	ANI30	00H	00H	●	-	-
	KR1	00H	00H	●	-	-
	SDI21	00H	00H	●	-	-
	SDA21	00H	00H	●	-	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	-	-
P72	GPIO	00H	00H	●	●	●
	ANI31	00H	00H	●	●	●
	KR2	00H	00H	●	●	-
	SDO21	00H	00H	●	-	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P73	GPIO	00H	00H	●	●	●
	ANI32	00H	00H	●	●	●
	KR3	00H	00H	●	●	-
	SDO01	00H	00H	●	●	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P74	GPIO	00H	00H	●	●	●
	ANI33	00H	00H	●	●	●
	KR4	00H	00H	●	●	-
	SDI01	00H	00H	●	●	-
	SDA01	00H	00H	●	●	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P75	GPIO	00H	00H	●	●	-
	ANI34	00H	00H	●	●	-
	KR5	00H	00H	●	●	-

	SCLK01	00H	00H	●	●	-
	SCL01	00H	00H	●	●	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	-
P120	GPIO	00H	00H	●	●	●
	ANI14	00H	00H	●	●	●
	VCOUT0	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P121	GPIO	00H	00H	●	●	●
	X1	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P122	GPIO	00H	00H	●	●	●
	X2	00H	00H	●	●	●
	EXCLK	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P123	GPIO	00H	00H	●	●	-
	XT1	00H	00H	●	●	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	-
P124	GPIO	00H	00H	●	●	-
	XT2	00H	00H	●	●	-
	EXCLKS	00H	00H	●	●	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	-
P130	GPIO	00H	00H	●	-	-
	ANI35	00H	00H	●	-	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	-	-
P136	GPIO	00H	00H	●	●	●
	ANI36	00H	00H	●	●	●
	INTP0	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P137	GPIO	00H	00H	●	●	●
	SWCLK	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
P140	GPIO	00H	00H	●	●	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	-
P146	GPIO	00H	00H	●	-	-
	ANI15	00H	00H	●	-	-
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	-	-
P147	GPIO	00H	00H	●	●	●
	ANI12	00H	00H	●	●	●
	VREF0	00H	00H	●	●	●
	Digital function	X（Refer to table 4.1.2）	X（Refer to table 4.1.2）	●	●	●
VDD	Power	-	-	●	●	●
VSS	Ground	-	-	●	●	●

All ports of this product are divided into 3 types, namely type 1 to type 3. The corresponding conditions are as follows:

Type 1: bidirectional I / O function

Type 2: only input function, such as clock, corresponding pins p121-p124

Type 3: reset function, corresponding to pin resetb

Refer to 4.3 port type for the block diagram of each type of pin

Table 4.1.2 Table of Digital function configuration（1/2 output functions）

Port Name	Configuration register	Setting value	Digital functions
P00~P147	P00cfg[3:0]~P147cfg[3:0]	4'h00	Default function
		4'h01	TO10
		4'h02	TO11
		4'h03	TO12
		4'h04	TO13
		4'h05	SDO00/TxD0
		4'h06	SDO20/TxD2
		4'h07	CLKBUZ0
		4'h08	SCLKO00
		4'h09	SCLKO20
		4'h0a	TxD1

Note： P60 and p61 are nod outputs, which should be noted during configuration and use.

Table 4.1.2 Table of Digital function configuration（2/2 input functions）

Configuration register	Setting value	Digital functions
TI10PCFG	6'h00	Default input function
TI11PCFG	6'h01	P00 selected as input function
TI12PCFG	6'h02	P01 selected as input function
TI13PCFG	6'h03	P10 selected as input function
INTP0PCFG	6'h04	P11 selected as input function
INTP1PCFG	6'h05	P12 selected as input function
INTP2PCFG	6'h06	P13 selected as input function
INTP3PCFG	6'h07	P14 selected as input function
SDI00PCFG (SPI/IIC/UART)	6'h08	P15 selected as input function
SCLKI00PCFG (SPI/IIC)	6'h09	P16 selected as input function
SS00PCFG (SPI)	6'h0a	P17 selected as input function
SDI20PCFG (SPI/UART)	6'h0b	P20 selected as input function
SCLKI20PCFG (SPI)	6'h0c	P21 selected as input function
RXD1PCFG (UART)	6'h0d	P22 selected as input function
SDAA0PCFG	6'h0e	P23 selected as input function
SCLA0PCFG	6'h0f	P24 selected as input function
	6'h10	P25 selected as input function
	6'h11	P26 selected as input function
	6'h12	P27 selected as input function

	6'h13	P30 selected as input function
	6'h14	P31 selected as input function
	6'h15	P40 selected as input function
	6'h16	P41 selected as input function
	6'h17	P50 selected as input function
	6'h18	P51 selected as input function
	6'h19	P60 selected as input function
	6'h1a	P61 selected as input function
	6'h1b	P62 selected as input function
	6'h1c	P63 selected as input function
	6'h1d	P70 selected as input function
	6'h1e	P71 selected as input function
	6'h1f	P72 selected as input function
	6'h20	P73 selected as input function
	6'h21	P74 selected as input function
	6'h22	P75 selected as input function
	6'h23	P120 selected as input function
	6'h24	P121 selected as input function
	6'h25	P122 selected as input function
	6'h26	P123 selected as input function
	6'h27	P124 selected as input function
	6'h28	P130 selected as input function
	6'h29	P136 selected as input function
	6'h2a	P136 selected as input function
	6'h2b	P140 selected as input function
	6'h2c	P146 selected as input function
	6'h2d	P147 selected as input function

Table 4.1.3 SPI pin function configuration register

Register name	Setting value	SPI pin function			
		SPINSS	SPISCK	SPIMISO	SPIMOSI
SPIPCFG[1:0]	2'b00	Not assigned to any pin			
	2'b01	P50	P51	P17	P16
	2'b10	P63	P31	P75	P74
	1'b11	P25	P24	P23	P22

4.2 Pins Other Than Port Pins

(1/2)

Function Name	I/O	Function
ANI0～ANI36	I	A/D converter analog input
INTP0～INTP3	I	External interrupt request input pin for which the valid edge (rising edge, falling edge, or both rising and falling edges) can
VCIN0	I	Comparator 0 analog voltage input
VCIN10, VCIN11, VCIN12, VCIN13	I	Comparator 1 analog voltage input/reference voltage input
VREF0	I	Comparator 0 reference voltage input
VCOUT0, VCOUT1	O	Comparator output
PGA0IN, PGA1IN	I	PGA voltage input
PGA0GND, PGA1GND	I	PGA reference voltage input
KR0 ～KR5	I	Key interrupt input
CLKBUZ0, CLKBUZ1	O	Clock output/buzzer output
RTC1HZ	O	Real-time clock correction clock (1 Hz) output
RESETB	I	This is the active-low system reset input pin. If it is not used, connect this pin to VDD through a resistor or directly.
IrRxD	I	IrDA receive data
IrTxD	O	IrDA transmit data
RxD0～RxD2	I	Serial data input pins of serial interface UART0 to UART2
TxD0～TxD2	O	Serial data output pins of serial interface UART0 to UART2
SCL00、SCL01、SCL10、SCL11、SCL20、SCL21	I/O	Serial clock I/O pins of serial interface IIC00, IIC01, IIC10, IIC11, IIC20 and IIC21
SDA00、SDA01、SDA10、SDA11、SDA20、SDA21	I/O	Serial data I/O pins of serial interface IIC00, IIC01, IIC10, IIC11, IIC20 and IIC21
SCLK00, SCLK01, SCLK10, SCLK11, SCLK20, SCLK21	I/O	Serial clock I/O pins of serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, and SSPI21
SDI00, SDI01, SDI10, SDI11, SDI20, SDI21	I	Serial data input pins of serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, and SSPI21

(2/2)

Function Name	I/O	Function
SS00	I	Chip select input pin of serial interface SSPI00
SDO00, SDO01, SDO10, SDO11, SDO20, SDO21	O	Serial data output pins of serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, and SSPI21
SCLA0	I/O	Serial clock I/O pins of serial interface IICA0
SDAA0	I/O	Serial data I/O pins of serial interface IICA0
SPINSS	I	Chip select input pin of serial interface SPI
SPISCK	I/O	Serial clock I/O pins of serial interface SPI
SPIMISO	I/O	Serial data input/output pins of serial interface SPI
SPIMOSI	I/O	Serial data input/output pins of serial interface SPI
TI00～TI03	I	The pins for inputting an external count clock/capture trigger
TO00～TO03	O	Timer output pins of 16-bit Timer4
TI10～TI13	I	The pins for inputting an external count clock/capture trigger
TO10～TO13	O	Timer output pins of 16-bit Timer4
X1, X2	-	Resonator connection for main system clock
EXCLK	I	External clock input for main system clock
XT1, XT2	-	Resonator connection for subsystem clock
EXCLKS	I	External clock input for subsystem clock
VDD	-	Positive power supply
AVREFP	I	A/D converter reference potential (+ side) input
AVREFM	I	A/D converter reference potential (- side) input
VSS	-	Ground
SWDIO	I/O	SWD data line
SWCLK	I	SWD clock line

Remark：Use bypass capacitors (about 0.1 uF) as noise and latch up countermeasures with relatively thick wires at the shortest distance to VDD to VSS lines.

5 Functional Overview

5.1 ARM® Cortex®-M0+ Core with MPU

Cortex-M0(+) processor is a new generation of ARM processors for embedded systems. It provides a low-cost platform for low pin count and low power consumption microcontrollers, while providing excellent computing performance and advanced system response to interrupts.

The 32-bit RISC processor of the Cortex-M0(+) processor provides excellent code efficiency and provides high-performance expectations of the ARM core, which is different from 8-bit and 16-bit devices of the same memory size. The Cortex-M0(+) processor has 32 address lines and a storage space of up to 4G.

BAT32G135 uses an embedded ARM core, so it is compatible with all ARM tools and software.

5.2 Memory

5.2.1 Flash

The MCU provides an on-chip flash memory support to program, erase and rewrite. Functions is shown in below:

- 64KB Flash Memory (program/data flash).
- 1.5 KB Special data flash memory
- Support sector erase, sector size is 512byte, erase time 4ms
- Support byte/half-word/word (32bit) programming, programming time 24us

5.2.2 SRAM

The MCU provides an on-chip high-speed SRAM module of 8KB with either parity-bit checking.

5.3 DMA

The built-in DMA (Direct Memory Access) controller can realize the function of data transfer between memories without using the CPU.

- Support the start of DMA through the interruption of peripheral functions, which can realize real-time control through communication, timer and A/D.
- Transfer space: 4 GB area from 0000 0000h to FFFF FFFFh except reserved areas.
- Support 4 transfer modes (normal transfer mode, repeat transfer mode, block transfer mode and chain transfer mode).

5.4 Event Link Controller (EVENTC)

The Event Link Controller (EVENTC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between the modules without CPU intervention.

The EVENTC has the following functions:

- Capable of directly linking event signals from 15 types of peripheral functions to specified peripheral functions.
- Event signals can be used as activation sources for operating any one of 3 types of peripheral functions.

5.5 Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.

The following three kinds of system clocks and clock oscillators are selectable.

5.5.1 Main System Clock

- X1 oscillator:
  This circuit oscillates a clock of fX = 1 to 20 MHz by connecting a resonator to X1 pin and X2 pin. Oscillation can be stopped by executing the DEEPSLEEP instruction or setting of the MSTOP bit.
- High-speed on-chip oscillator (High-speed OCO):
  The frequency at which to oscillate can be selected from among fHOCO = 64, 48, 32, 24, 16, 12, 8, 6, 4, 3, 2, or 1 MHz (TYP.) by using the option byte. After a reset release, the CPU always starts operating with this high-speed on-chip oscillator clock. Oscillation can be stopped by executing the DEEPSLEEP instruction or setting of the HIOSTOP bit. The frequency specified by using an option byte can be changed by using the high-speed on-chip oscillator frequency select register (HOCODIV).
- X2 external main system clock:
  An external main system clock (fEX = 1 to 20 MHz) can also be supplied from the EXCLK/X2/P122 pin. An external main system clock input can be disabled by executing the STOP instruction or setting of the MSTOP bit.

5.5.2 Subsystem Clock

- XT1 clock oscillator:
  This circuit oscillates a clock of fXT = 32.768 KHz by connecting a 32.768 KHz resonator to XT1 pin and XT2 pin. Oscillation can be stopped by setting the XTSTOP bit.
- XT2 external subsystem clock:
  An external subsystem clock (fEXS = 32.768 KHz) can also be supplied from the EXCLKS/XT2/P124 pin. An external subsystem clock input can be disabled by the setting of the XTSTOP bit.

5.5.3 Low-speed On-chip Oscillator

- Low-speed on-chip oscillator (Low-speed OCO):
  This circuit oscillates a clock of fIL = 15 KHz (TYP.).
  The low-speed on-chip oscillator clock cannot be used as the CPU clock.
  Only the following peripheral hardware runs on the low-speed on-chip oscillator clock.
  - Watchdog timer (WWDT)
  - Real-time clock (RTC)
  - 15-bit interval timer

5.6 Power Management

5.6.1 Power Supply

VDD: External power, voltage range 1.8 to 5.5V

5.6.2 Power-on-reset Circuit

The power-on-reset circuit (POR) has the following functions.

- Generates internal reset signal at power on. The reset signal is released when the supply voltage (VDD) exceeds the detection voltage (VPOR). Note that the reset state must be retained until the operating voltage becomes in the range defined of POR function. This can be achieved by utilizing the voltage detection circuit or controlling the externally input reset signal.
- Compares supply voltage (VDD) and detection voltage (VPDR), and then generates internal reset signal when VDD < VPDR. Note that, after power is supplied, this LSI should be placed in the DEEPSLEEP mode, or in the reset state by utilizing the voltage detector or externally input reset signal, before the operation voltage falls below the range defined of POR function. When restarting the operation, make sure that the operation voltage has returned within the range of operation.

5.6.3 Voltage Detector

The operation mode and detection voltages (VLVDH, VLVDL, VLVD) for the voltage detector is set by using the option byte. The voltage detector (LVD) has the following functions.

- The LVD circuit compares the supply voltage (VDD) with the detection voltage (VLVDH, VLVDL, VLVD), and generates an internal reset or internal interrupt signal.
- The detection level for the power supply detection voltage (VLVDH, VLVDL, VLVD) can be selected by using the option byte.
- Operable in DEEPSLEEP mode.
- When the power supply rises, before reaching the working voltage range, it must be kept in the reset state through the voltage detection circuit or external reset. When the power supply drops, it must be transferred to deep sleep mode before it is less than the operating voltage range, or set to the reset state by the voltage detection circuit or external reset.
- The range of operating voltage varies with the setting of the user option byte.

5.7 Low Power Modes

The product supports two low-power modes with short start-up time:

- SLEEP Mode: When a WFI instruction is executed while SBYCR.SSBY bit is 0, the MCU enters Sleep mode. In this mode, the CPU stops operating but the contents of its internal registers are retained. Other peripheral functions do not stop. Available resets or interrupts in Sleep mode cause the MCU to cancel Sleep mode.
- DEEPSLEEP Mode: When a WFI instruction is executed while SBYCR.SSBY bit is 1, the MCU enters Software Deepsleep mode. In this mode, the CPU, most of the on-chip peripheral functions and oscillators stop. However, the contents of the CPU internal registers and SRAM data, the states of on-chip peripheral functions and the I/O Ports are retained. Deepsleep mode allows a significant reduction in power consumption because most of the oscillators stop in this mode.

In either mode, the registers, flags, and data memory retain their contents before being set to standby mode, and also maintain the status of the output latch and output buffer of the input/output port.

5.8 Reset Function

The following seven operations are available to generate a reset signal.

1) External reset input via RESETB pin
2) Internal reset by watchdog timer program loop detection
3) Internal reset by comparison of supply voltage and detection voltage of power-on-reset (POR) circuit
4) Internal reset by comparison of supply voltage of the voltage detector (LVD) and detection voltage
5) Internal reset by RAM parity error
6) Internal reset by illegal-memory access
7) software reset

External and internal resets start program execution from the address at 0000H and 0001H when the reset signal is generated.

5.9 Interrupts

The Cortex-M0+ processor has a built-in Nested Vectored Interrupt Controller (NVIC) that supports up to 32 interrupt request (IRQ) inputs and one non-maskable interrupt (NMI) input. In addition, the processor supports multiple internal exceptions.

This product extends 32 maskable interrupt requests (IRQ) and 1 non-maskable interrupt (NMI), and can support up to 64 maskable interrupt sources and one non-maskable interrupt source. The actual number of interrupt sources varies by product.

5.10 Real-timer Clock (RTC)

The real-time clock has the following features.

- Counters of year, month, week, day, hour, minute, and second.
- Constant-period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm: week, hour, minute)
- Pin output function of 1 Hz
- Support frequency division of sub-system clock or main system clock as RTC running clock
- Real-time clock interrupt signal (INTRTC) can be used to wake up in deep sleep mode
- Support a wide range of clock correction functions

Caution: The count of year, month, week, day, hour, minutes and second can only be performed when a subsystem clock (fSUB = 32.768 KHz) is selected as the operation clock of the real-time clock.

When the low-speed oscillation clock (fIL = 15 KHz/30KHz) is selected, only the constant-period Interrupt function is available.

5.11 Watchdog Timer

The counting operation of the watchdog timer is set by the option byte. The watchdog timer operates on the low-speed on-chip oscillator clock (fIL = 15 KHz). The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

Program loop is detected in the following cases:

- If the watchdog timer counter overflows
- If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
- If data other than “ACH” is written to the WDTE register
- If data is written to the WDTE register during a window close period

5.12 SysTick Timer

This timer is dedicated to real-time operating systems, but can also be used as a standard down counter.

Its characteristics are: when the 24-bit down counter self-loading capacity counter reaches 0, there is a shieldable system interruption.

5.13 Timer4

The timer4 has eight (two units of four) 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more “channels” can be used to create a high-accuracy timer.

For details about each function, see the table below.

Independent channel operation function	Simultaneous channel operation function
● Interval timer ● Square wave output ● External event counter ● Divider ● Input pulse interval measurement ● Measurement of high-/low-level width of input signal ● Delay counter	● One-shot pulse output ● PWM output ● Multiple PWM output

5.13.1 Independent Channel Operation Function

By operating a channel independently, it can be used for the following purposes without being affected by the operation mode of other channels.

1) Interval timer: Each timer of the unit can be used as a reference timer that generates an interrupt (INTTM) at fixed intervals.
2) Square wave output: A toggle operation is performed each time INTTMmn interrupt is generated and a square wave with a duty factor of 50% is output from a timer output pin (TO).
3) External event counter: Each timer of the unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TI) has reached a specific value.
4) Divider function (channel 0 only): A clock input from a timer input pin (TI00) is divided and output from an output pin (TO00).
5) Input pulse interval measurement: Counting is started by the valid edge of a pulse signal input to a timer input pin (TI). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.
6) Measurement of high-/low-level width of input signal: Counting is started by a single edge of the signal input to the timer input pin (TI), and the count value is captured at the other edge. In this way, the high-level or low-level width of the input signal can be measured.
7) Delay counter: Counting is started at the valid edge of the signal input to the timer input pin (TI), and an interrupt is generated after any delay period.

5.13.2 Simultaneous Channel Operation Function

By using the combination of a master channel (a reference timer mainly controlling the cycle) and slave channels (timers operating according to the master channel), channels can be used for the following purposes.

1) One-shot pulse output: Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width.
2) PWM (Pulse Width Modulation) output: Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.
3) Multiple PWM (Pulse Width Modulation) Outputs: Up to 3+3 PWM signals of arbitrary duty cycle can be generated at a fixed period by expanding the PWM function and using one master channel and multiple slave channels.

5.13.3 8-bit Timer Operation Function

The 8-bit timer operation function makes it possible to use a 16-bit timer channel in a configuration consisting of two 8-bit timer channels. This function can only be used for channels 1 and 3.

5.13.4 LIN-bus supporting function

Timer4 is used to check whether signals received in LIN-bus communication match the LIN-bus communication format.

1) Detection of wakeup signal: The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD0) of UART0 and the count value of the timer is captured at the rising edge. In this way, a low-level width can be measured. If the low-level width is greater than a specific value, it is recognized as a wakeup signal.
2) Detection of break field: The timer starts counting at the falling edge of a signal input to the serial data input pin (RxD0) of UART0 after a wakeup signal is detected, and the count value of the timer is captured at the rising edge. In this way, a low-level width is measured. If the low-level width is greater than a specific value, it is recognized as a break field.
3) Measurement of pulse width of sync field: After a break field is detected, the low-level width and high-level width of the signal input to the serial data input pin (RxD0) of UART0 are measured. From the bit interval of the sync field measured in this way, a baud rate is calculated.

5.14 EPWM Outpu Control Function

Use Timer4's PWM output function to control one DC motor or two stepping motors. By truncating the source CMP0 output, INTP0 input and EVENTC event, the output can be truncated. Through the setting of the software, it is possible to choose from 4 types of output for Hi-Z output, low-level output, high-level output and forbidden cut-off output.

5.15 15-bit Interval Timer

An interrupt (INTIT) is generated at any previously specified time interval. It can be utilized for wakeup from DEEPSLEEP mode.

5.16 Clock Output/Buzzer Output Controller

The clock output controller is intended for clock output for supply to peripheral ICs. Buzzer output is a function to output a square wave of buzzer frequency.

5.17 Serial communication Interface (SCI)

This product has two serial array units. Serial array unit has four serial channels. All channels can achieve UART, simplified SPI (3-wire serial) and simplified I2C.Function assignment of each channel is as shown below.

5.17.1 3-wire Serial I/O (SSPI)

Data is transmitted or received in synchronization with the serial clock (SCK) output from the master channel.3-wire serial communication is clocked communication performed by using three communication lines: one for the serial clock (SCK), one for transmitting serial data (SO), one for receiving serial data (SI).

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate

During master communication: Max. fCLK/2

During slave communication: Max. fMCK/6

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

5.17.2 4-wire Serial I/O with Slave Select Input Function

This is a clock synchronization using a slave chip select input (SSI), a serial clock (SCK), a transmit serial data (SO) and a receive serial data (SI) a total of 4 communication lines for communication Communication Interface.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate

During slave communication: Max. fMCK/6

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

5.17.3 UART

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception(RxD) lines. By using these two communication lines, each data frame, which consist of start bit, data, parity bit and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using UART0, Timer4 unit 0 (channel 3), and an external interrupt (INTP0).

[Data transmission/reception]

- Data length of 7, 8, or 9 bits
- Select the MSB/LSB first
- Level setting of transmit/receive data (selecting whether to reverse the level)
- Parity bit appending and parity check functions
- Stop bit appending, stop bit check function

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]

- Framing error, parity error, or overrun error

[LIN-bus functions]

- Wakeup signal detection
- Break field (BF) detection
- Sync field measurement, baud rate calculation

5.17.4 Simplified I²C

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This simplified I2C is designed for single communication with a device such as EEPROM, flash memory, or A/D converter, and therefore, it functions only as a master. Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

[Data transmission/reception]

- Master transmission, master reception (only for single master application)
- ACK output function and ACK detection function
- Data length of 8 bits (When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Manual generation of start condition and stop condition

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

- ACK error or overrun error

[Functions not supported by simplified I2C]

- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection functions

5.18 Standard Serial Peripheral Interface SPI

The serial interface SPI has the following 2 modes.

- Operation stop mode:
  This mode is used when serial transfers are not performed. It can reduce power consumption.
- 3-wire serial I/O mode:
  This mode uses 3 lines of serial clock (SCK) and serial data bus (MISO and MOSI) to transmit 8-bit or 16-bit data with multiple devices.

5.19 Serial Interface IICA

Serial interface IICA has the following three modes.

- Operation stop mode:
  This mode is used when serial transfers are not performed. It can reduce power consumption.
- I2C bus mode (multi-master application supported):
  This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLAn) line and a serial data bus (SDAAn) line.
  It complies with the I2C bus format and the master device can generate “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. It can simplify the part of application program that controls the I2C bus. Since the SCLA and SDAA pins are used for open drain outputs, serial interface IICA requires pull-up resistors for the serial clock line and the serial data bus line.
- Wakeup mode:
  The DEEPSLEEP mode can be released by generating an interrupt request signal (INTIICA) when an extension code from the master device or a local address has been received while in DEEPSLEEP mode.

5.20 A/D Converter (ADC)

The A/D converter is a converter that converts analog input signals into digital values, and is configured to control analog inputs, including up to 35 channels of A/D converter analog inputs (ANI0 to ANI13, ANI16 to ANI36).

The A/D converter has the following function.

- 12-bit resolution A/D conversion, Conversionrate 1.42Msps.
- Trigger mode: Software trigger, Hardware trigger mode
- Channel selection: Sigle channel select mode and Scan mode
- Conversion operation mode: One-shot conversion mode and Sequential conversion mode
- Operation voltage:1.8V≤VDD≤5.5V
- Can detect the internal reference voltage (1.45V) and temperature sensor.

Various A/D conversion modes can be specified by using the mode combinations below.

Trigger mode	Software trigger	Conversion is started by software.
	Hardware trigger no-wait mode	Conversion is started by detecting a hardware trigger.
	Hardware trigger wait mode	The power is turned on by detecting a hardware trigger while the system is off and in the conversion standby state, and conversion is then started automatically after the stabilization wait time passes.
Channel selection mode	Select mode	A/D conversion is performed on the analog input of one selected channel.
	Scan mode	A/D conversion is performed on the analog input of four channels in order. Four consecutive channels can be selected from ANI0 to ANI15 as analog input channels.
Conversion operation mode	One-shot conversion mode	A/D conversion is performed on the selected channel once.
	Sequential conversion mode	A/D conversion is sequentially performed on the selected channels until it is stopped by software.
Sampling time/ Conversion time	Sampling clock cycles / Conversion clock cycles	The sampling time can be set by the register. The default value of the sampling clock is 13.5 clk, and the conversion clock number Min is 31.5 clk.

5.21 Programmable Gain Amplifier (PGA)

This product has two programmable gain amplifiers (PGA0, PGA1), The programmable gain amplifier is provided with the following functions.

- GAIN: X4, X8, X10, X12, X14, X16, X32
- The external pin(PGAGND) can be selected as the ground of the negative feedback resistance of the PGA (can be used as a differential mode)
- The output of PGA0 can be selected as the analog input for the A/D converter or the analog input of the positive terminal of comparator 0 (CMP0)
- PGA1 output can be selected as analog input for A/D converter

5.22 Comparator (CMP)

The product has two comparator channels. The comparator has the following functions.

- A pin selector switch is added to the analog input of CMP1.
- The external reference voltage input or internal reference voltage can be selected as the reference voltage.
- The canceling width of the noise canceling digital filter can be selected.
- An interrupt signal can be generated by detecting an active edge of the comparator output.
- An event link controller (EVENTC) event signal can be output by detecting an active edge of the comparator output.

5.23 Serial Wire Debug (SW-DP)

SW-DP interface allows connection to the microcontroller via serial line debugging tools.

5.24 Safety Functions

5.24.1 Flash Memory CRC Operation Function (High-speed CRC, General-purpose CRC)

This detects data errors in the flash memory by performing CRC operations.

Two CRC functions are provided according to the different applications.

- High-speed CRC: The CPU can be stopped and a high-speed check executed on its entire code flash memory area during the initialization routine.
- General CRC: This can be used for checking various data in addition to the code flash memory area while the CPU is running.

5.24.2 RAM Parity Error Detection Function

This detects parity errors when the RAM is read as data.

5.24.3 SFR Guard Function

This prevents SFRs (Special Function Register) from being rewritten when the CPU freezes.

5.24.4 Invalid Memory Access Detection Function

This detects illegal accesses to invalid memory areas.

5.24.5 Frequency Detection Function

This uses the timer4 to perform a self-check of the CPU/peripheral hardware clock frequency.

5.24.6 A/D Test Function

This is used to perform a self-check of A/D converter by performing A/D conversion on the positive internal reference voltage, negative reference voltage, analog input channel (ANI), temperature sensor output, and internal reference voltage output.

5.24.7 Digital Output Signal Level Detection Function

When the I/O pins are output mode, the output level of the pin can be read.

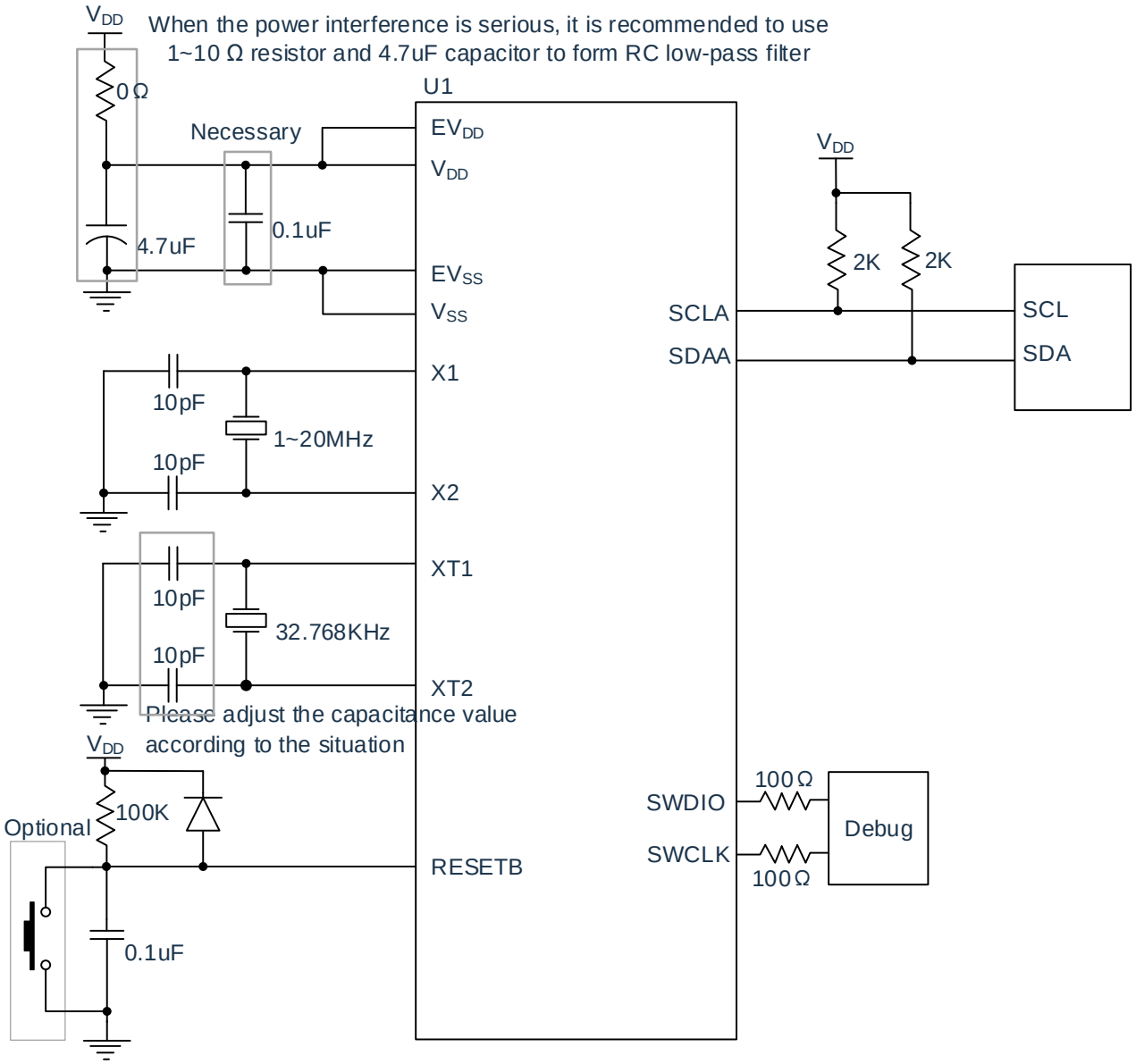
5.25 Key Function

A key interrupt (INTKR) can be generated by inputting a falling edge to the key interrupt input pins (KR0 to KR5).

6 Electrical Characteristics

6.1 Typical Application Peripheral Circuit

The connection reference of the MCU typical application peripheral circuit is as follows:



6.2 Absolute Maximum Voltage Ratings

(TA=–40～+105°C)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	VDD		–0.5～+6.5	V
Input voltage	VI1	P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P62～P63、P70～P75、P120～P124、P130、P136、P137、P140、P146、P147、EXCLK、EXCLKS、RESETB	–0.3～VDD+0.3 note1	V
	VI2	P60～P61(N channel drain open circuit）	－0.3～+6.5	V
Output voltage	VO	P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P60～P63、P70～P75、P120、P130、P136、P137、P140、P146、P147	–0.3～VDD+0.3 note1	V
Analog input voltage	VAI	ANI0～ANI24、ANI27～ANI36	–0.3～VDD+0.3 and –0.3～AVREF(+)+0.3 note1, 2	V

note:

1. Must be 6.5 V or lower.
2. Do not exceed AVREF (+) + 0.3 V in case of A/D conversion target pin.

Caution:

Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark:

1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
2. AVREF (+): + side reference voltage of the A/D converter.
3. VSS: Reference voltage

6.3 Absolute Maximum Current Ratings

(TA=–40～+105°C)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P62～P63、P70～P75、P130、P136、P137、P140、P146、P147	-40	mA
		Total of all pins	P00～P01、P20～P27、P40～P41、P120、P130、P136、P137、P140	-70	mA
			P10～P17、P30～P31、P50～P51、P62～P63、P70～P75、P146、P147	-100	mA
	IOH2	Per pin	P121～P124	-3	mA
		Total of all pins		-15	mA
Output current, low	IOL1	Per pin	P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P60～P63、P70～P75、P120、P130、P136、P137、P140、P146、P147	40	mA
		Total of all pins	P00～P01、P20～P27、P40～P41、P120、P130、P136、P137、P140	100	mA
			P10～P17、P30～P31、P50～P51、P60～P63、P70～P75、P146、P147	120	mA
	IOL2	Per pin	P121～P124	15	mA
		Total of all pins		45	mA
Operating ambient temperature	TA	In normal operation mode		–40～+105	°C
		In flash memory programming mode			
Storage temperature	Tstg			–65～+150	°C

Caution:

Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark:

Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

6.4 Oscillator Characteristics

6.4.1 X1, XT1 Characteristics

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

Resonator	Resonator	Conditions	MIN	TYP	MAX	Unit
X1 clock oscillation frequency (fX)	Ceramic resonator/ crystal resonator		1.0	-	20.0	MHz
X1 clock oscillation stabilization time	Ceramic resonator/ crystal resonator	20MHz，C=10pF		15		ms
X1 clock oscillation feedback resistor	Ceramic resonator/ crystal resonator		0.6		1.8	MΩ
XT1 clock oscillation frequency (fXT)	Crystal resonator		32	32.768	35	KHz
XT1 clock oscillation stabilization time	Crystal resonator	32.768KHz，C=10pF		2		s

Note:
Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time.
Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

6.4.2 On-chip Oscillator Characteristics

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

Oscillators	Conditions	MIN	TYP	MAX	Unit
High-speed on-chip oscillator clock frequency(fIH) Notes 1, 2		1.0		64.0	MHz
High-speed on-chip oscillator stabilization time(tSU)			12		us
High-speed on-chip oscillator clock frequency accuracy	TA= 10～+105℃	-1.0		+1.0	%
	TA= -10～+105℃	-1.5 Note3		-1.5 Note3	%
	TA=–40～+105℃	-4.0Note3		-4.0Note3	%
Low-speed on-chip oscillator clock frequency(fIL)		10	15	20	KHz

Note:
1. High-speed on-chip oscillator frequency is selected with the option byte and HOCODIV register.
2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.
3. The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured for mass production.

6.5 DC Characteristics

6.5.1 Pin Characteristics

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS= 0V)

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
Output current, high Note 1	IOH1	Per pin for P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P62～P63、P70～P75、P120、P130、P136、P137、P140、P146、P147	1.8V≤VDD≤5.5V –40～+85℃			-12.0Note2	mA
			1.8V≤VDD≤5.5V 85～+105℃			-6.0Note2	
		Total of P00～P01、P20～P27、P40～P41、P120、P130、P136、P137、P140 (When duty ≤ 70% Note 3)	4.0V≤VDD≤5.5V –40～+85℃			-60.0	mA
			4.0V≤VDD≤5.5V 85～+105℃			-30.0	
			2.4V≤VDD＜4.0V			-12.0	mA
			1.8V≤VDD＜2.4V			-6.0	mA
		Per pin for P10～P17、P30～P31、P50～P51、P62～P63、P70～P75、P146、P147 (When duty ≤ 70% Note 3)	4.0V≤VDD≤5.5V –40～+85℃			-80.0	mA
			4.0V≤VDD≤5.5V 85～+105℃			-30.0	
			2.4V≤VDD＜4.0V			-20.0	mA
			1.8V≤VDD＜2.4V			-10.0	mA
		Total (When duty ≤ 70% Note 3)	1.8V≤VDD≤5.5V –40～+85℃			-140.0	mA
			1.8V≤VDD≤5.5V 85～+105℃			-60.0	mA
	IOH2	Per pin for P121 ～ P124	1.8V≤VDD≤5.5V			-2.5note2	mA
		Total of P121 ～ P124 (When duty ≤ 70% Note 3)	1.8V≤VDD≤5.5V			-10	mA

Note:

1. Value of current at which the device operation is guaranteed even if the current flows from the VDD pins to an output pin.
2. Do not exceed the total current value.
3. Specification under conditions where the duty factor ≤ 70%.
   The output current value that has changed to the duty factor ＞ 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current of pins = (IOH × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOH = -10.0 mA

Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark: Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
Output current, low Note 1	IOH1	Per pin for P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P60～P63、P70～P75、P120、P130、P136、P137、P140、P146、P147	1.8V≤VDD≤5.5V –40～+85℃			35 note2	mA
			1.8V≤VDD≤5.5V 85～+105℃			20 note2	
		Total of P00～P01、P20～P27、P40～P41、P120、P130、P136、P137、P140 (When duty ≤ 70% Note 3)	4.0V≤VDD≤5.5V –40～+85℃			100	mA
			4.0V≤VDD≤5.5V 85～+105℃			70	
			2.4V≤VDD＜4.0V			30	mA
			1.8V≤VDD＜2.4V			15	mA
		Per pin for P10～P17、P30～P31、P50～P51、P60～P63、P70～P75、P146、P147 (When duty ≤ 70% Note 3)	4.0V≤VDD≤5.5V –40～+85℃			120	mA
			4.0V≤VDD≤5.5V 85～+105℃			80	
			2.4V≤VDD＜4.0V			40	mA
			1.8V≤VDD＜2.4V			20	mA
		Total (When duty ≤ 70% Note 3)	1.8V≤VDD≤5.5V –40～+85℃			150	mA
			1.8V≤VDD≤5.5V 85～+105℃			100	mA
	IOH2	Per pin for P121 ～ P124	1.8V≤VDD≤5.5V			10 note2	mA
		Total of P121 ～ P124 (When duty ≤ 70% Note 3)	1.8V≤VDD≤5.5V			40	mA

Note:

1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pins.
2. Do not exceed the total current value.
3. Specification under conditions where the duty factor ≤ 70%.
   The output current value that has changed to the duty factor ＞ 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark: Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
Power input voltage	VDD EVDD			1.8		5.5	V
Power supply ground input voltage	VSS EVSS			-0.3			V
Input voltage, high	VIH1	P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P62～P63、P70～P75、P120～P124、EXCLK、EXCLKS、RESETB、P130、P136、P137、P140、P146、 P147	Schmitt input	0.8VDD		VDD	V
	VIH2	P60～P61		0.7VDD		6.0	
Input voltage, low	VIL1	P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P62～P63、P70～P75、P120～P124、EXCLK、EXCLKS、RESETB、P130、P136、P137、P140、P146、 P147	Schmitt input	0		0.2VDD	V
	VIL2	P60～P61		0		0.3VDD	V

Remark: Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA=–40 ～ +105℃, 1.8V≤EVDD=VDD≤5.5V, VSS=Evss=0V)

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
Output voltage, high	VOH1	P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P62～P63、 P70～P75、P120、P130、P136、P137、P140、P146、P147	4.0V≤VDD≤5.5V、IOH1=–12.0mA	VDD–1.5			V
			4.0V≤VDD≤5.5V、IOH1=–6.0mA	VDD–0.7			V
			2.4V≤VDD≤5.5V、IOH1=–3.0mA	VDD–0.6			V
			1.8V≤VDD≤5.5V、IOH1=–2mA	VDD–0.5			V
	VOH2	P121～P124	4.0V≤VDD≤5.5V、IOH2=–2.5mA	VDD–1.5			V
			4.0V≤VDD≤5.5V、IOH2=–1.5mA	VDD–0.7			V
			2.4V≤VDD≤5.5V、IOH2=–0.5mA	VDD–0.6			V
			1.8V≤VDD≤5.5V、IOH2=–0.4mA	VDD–0.5			V
Output voltage, low	VOL1	P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P60～P63、 P70～P75、P120、P130、P136、P137、P140、P146、P147	4.0V≤VDD≤5.5V、IOL1=35.0mA			1.2	V
			4.0V≤VDD≤5.5V、IOL1=20.0mA			0.7	V
			2.4V≤VDD≤5.5V、IOL1=9.0mA			0.4	V
			1.8V≤VDD≤5.5V、IOL1=6.0mA			0.4	V
	VOL2	P121～P124	4.0V≤VDD≤5.5V、IOL2=10.0mA			1.2	V
			4.0V≤VDD≤5.5V、IOL2=6.0mA			0.7	V
			2.4V≤VDD≤5.5V、IOL2=2.5mA			0.4	V
			1.8V≤VDD≤5.5V、IOL2=1.5mA			0.4	V

Remark: Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS= 0V)

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
Input leakage current, high	ILIH1	P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P60～P63、P70～P75、P120、P130、P136、P137、P140、P146、P147	VI=VDD			1	μA
	ILIH2	RESETB	VI=VDD			1	μA
	ILIH3	P121～P124 （X1、X2、EXCLK、XT1、XT2、EXCLKS）	VI=VDD, In input port or external clock input			1	μA
			VI=VDD, In resonator connection			10	μA
Input leakage current, low	ILIL1	P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P60～P63、P70～P75、P120、P130、P136、P137、P140、P146、P147	VI=VSS			-1	μA
	ILIL2	RESETB	VI=VSS			-1	μA
	ILIL3	P121～P124 （X1、X2、EXCLK、XT1、XT2、EXCLKS）	VI=VSS, In input port or external clock input			-1	μA
			VI=VSS, In resonator connection			-10	μA
On-chip pull-up resistance	RU	P00～P01、P10～P17、P20～P27、P30～P31、P40～P41、P50～P51、P62～P63、P70～P75、P120、P130、P136、P137、P140、P146、P147	VI=VSS, In input port	10	30	100	kΩ
On-chip pull-down resistance	RD	P00～P01、P10～P17、P20～P27、P30～P31、P50～P51、P62～P63、P70～P75、P120、P130、P136、P137、P140、P146、P147	VI=VDD, In input port	10	30	100	kΩ

Remark: Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

6.5.2 Supply Current Characteristics

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}= 0V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	High-speed on-chip oscillator	f_{HOCO}=64MHz, f_{IH}=64MHz note3			2.4	6.9	mA
				f_{HOCO}=32MHz, f_{IH}=32MHz note3			1.6	4.6	
			high-speed main clock	f_{MX}=20MHz note2	Square wave		1.0	3.1	mA
					Resonator		1.0	3.1	
			high-speed SUB clock	f_{SUB}=32.768KHz note4	Square wave		70	85	uA
					Resonator		70	85	
			Low-speed on-chip oscillator	fIL=15KHz Note8			70	85	uA
	I_{DD2}	Sleep mode	High-speed on-chip oscillator	f_{HOCO}=64MHz, f_{IH}=64MHz note3			1.8	4.0	mA
				f_{HOCO}=32MHz, f_{IH}=32MHz note3			1.2	2.6	
			high-speed main clock	f_{MX}=20MHz note2	Square wave		0.7	1.8	mA
					Resonator		0.7	1.8	
			high-speed SUB clock	f_{SUB}=32.768KHz note5	Square wave		0.7	12.5	uA
					Resonator		0.7	12.5	
			Low-speed on-chip oscillator	fIL=15KHz Note8			0.9	13	
	I_{DD3} note6	Deep Sleep mode note7	T_A=–40℃~+25℃ VDD=3.0V				0.45	1.0	uA
			T_A=–40℃~+85℃ VDD=3.0V				0.45	7.5	
			T_A=–40℃~+105℃ VDD=3.0V				0.45	12.5	

Note:

1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The values of the TYP. column include the current of the CPU executing the multiplication instruction (IDD1), not including the peripheral operation current. The values below the MAX. column include the current of the CPU executing the multiplication instruction (IDD1) and the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
2. When high-speed on-chip oscillator and subsystem clock are stopped.
3. When high-speed system clock and subsystem clock are stopped.
4. When high-speed on-chip oscillator and high-speed system clock are stopped.
5. When high-speed on-chip oscillator and high-speed system clock are stopped. The current flowing into the RTC is included.
6. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
7. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
8. Regarding the value for current to operate the subsystem clock in DeepSleep mode, refer to that in Sleep mode.

9. When high-speed on-chip oscillator, high-speed system clock and subsystem clock are stopped.

Remark:

1. fHOCO: High-speed on-chip oscillator clock frequency. fIH: High-speed on-chip oscillator systerm clock frequency.
2. fSUB: Subsystem clock frequency (XT1/XT2 clock oscillation frequency).
3. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency).
4. fIL: Low-speed on-chip oscillator systerm clock frequency.
5. Temperature condition of the TYP. value is TA = 25℃.

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS= 0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL note1				0.2		uA
RTC operating current	IRTC note1,2,3				0.04		uA
15-bit interval timer operating current	IIT note1,2,4				0.02		uA
Watchdog timer operating current	IWDT note1,2,5	fIL=15KHz			0.22		uA
A/D operating current	IADC note1,6	ADC HS mode@64MHz			2.2		mA
		ADC HS mode @4MHz			1.3		mA
		ADC LC mode @24MHz			1.1		mA
		ADC LC mode @4MHz			0.8		mA
PGA operating current		Per PGA channel			480	700	uA
CMP operating current	ICMP note1,9	Per CMP channel	When the internal reference voltage is not in use		60	100	uA
			When the internal reference voltage is in use		80	140	uA
LVD operating current	ILVD note1,7				0.08		uA

Note:

1. Current flowing to VDD.
2. When high speed on-chip oscillator and high-speed system clock are stopped.
3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator andthe XT1 oscillator). The supply current of the microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock operates in operation mode or Sleep mode. When the low-speed on-chip oscillator is selected, IFIL should be added. IDD2 subsystem clock operation includes the operational current of the real-time clock.
4. Current flowing only to the 15-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the microcontrollers is the sum of the values of either IDD1 or IDD2, and IIT, when the 15-bit interval timer operates in operation mode or Sleep mode. When the low-speed on-chip oscillator is selected, IFIL should be added.
5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip

oscillator).

6. Current flowing only to the A/D converter. The supply current of the microcontrollers is the sum of IDD1 or IDD2 and IADC when the A/D converter operates in an operation mode or the Sleep mode.
7. Current flowing only to the LVD circuit. The supply current of the microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.
8. Current flowing only to the D/A converter. The supply current of the microcontrollers is the sum of IDD1 or IDD2 and IDAC when the D/A converter operates in an operation mode or the Sleep mode.
9. Current flowing only to the comparator circuit. The supply current of the microcontrollers is the sum of IDD1, IDD2, or IDD3 and ICMP when the comparator circuit is in operation.

Remark:

1. fIL: Low-speed on-chip oscillator clock frequency
2. temperature condition of the TYP. value is TA = 25℃.

6.6 AC Characteristics

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}= 0V)

Items	Symbol	Conditions		MIN	TYP	MAX	Unit
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (fMAIN)operation	1.8V≤VDD≤5.5V	0.015625		1	us
		Subsystem clock (fSUB) operation	1.8V≤VDD≤5.5V	28.5	30.5	31.3	us
External system clock frequency	fEX	1.8V≤VDD≤5.5V		1.0		20.0	MHz
	fEXS	1.8V≤VDD≤5.5V		32.0		35.0	KHz
External system clock input high-level width, low-level width	tEXH, tEXL	1.8V≤VDD≤5.5V		24			ns
	tEXHS, tEXLS	1.8V≤VDD≤5.5V		13.7			us
TI00 ～ TI03, input high-level width, low-level width	tTIH, tTIL	1.8V≤VDD≤5.5V		1/fMCK+10			ns
TO00 ～ TO03, TO10 ～ T103, output frequency	fTO	4.0V≤VDD≤5.5V				16	MHz
		2.4V≤VDD＜4.0V				8	MHz
		1.8V≤VDD＜2.4V				4	MHz
CLKBUZ0, CLKBUZ1 output frequency	fPCL	4.0V≤VDD≤5.5V				16	MHz
		2.4V≤VDD＜4.0V				8	MHz
		1.8V≤VDD＜2.4V				4	MHz
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0 ～ INTP11	1.8V≤VDD≤5.5V	1			us
Key interrupt input low-level width	tKR	KR0 ～ KR5	1.8V≤VDD≤5.5V	250			ns
RESETB low-level width	tRSL			10			us

Remark: fMCK: timer4 operation clock frequency

6.7 Peripheral Functions Characteristics

6.7.1 Serial Communication Interface

1) UART mode

・(T_A=–40～+85℃, 1.8V≤VDD≤5.5V, V_{SS}= 0V)

Parameter	Conditions		Spec		Unit
			MIN	MAX	
Transfer rate	1.8V ≤VDD ≤ 5.5V			fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK=fCLK		10.6	Mbps

・(T_A=+85～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

Parameter	Conditions				Unit
			MIN	MAX	
Transfer rate	1.8V ≤VDD ≤ 5.5V			fMCK/12	bps
		Theoretical value of the maximum transfer rate fMCK=fCLK		5.3	Mbps

2) 3-wire serial I/O(SSPI) (master mode, internal clock output)

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

Parameter	Symbol	Conditions		–40 ～ +85℃		+85 ～ +105℃		Unit
				MIN	MAX	MIN	MAX	
SCLKp cycle time	tKCY1	tKCY1 ≥ 2/fCLK	4.0V ≤ VDD ≤ 5.5V	31.25		62.5		ns
			2.7V ≤ VDD ≤ 5.5V	41.67		83.3		
			2.4V ≤ VDD ≤ 5.5V	65		125		ns
			1.8V ≤VDD ≤ 5.5V	125		250		ns
SCLKp high-/low-level width	tKH1, tKL1	4.0V ≤ VDD ≤ 5.5V		tKCY1/2–4		tKCY1/2–7		ns
		2.7V ≤ VDD ≤ 5.5V		tKCY1/2–5		tKCY1/2–10		ns
		2.4V ≤ VDD ≤ 5.5V		tKCY1/2–10		tKCY1/2–20		ns
		1.8V ≤VDD ≤ 5.5V		tKCY1/2–19		tKCY1/2–38		ns
SDIp setup time (to SCLKp↑)	tSIK1	4.0V ≤ VDD ≤ 5.5V		12		23		ns
		2.7V ≤ VDD ≤ 5.5V		17		33		ns
		2.4V ≤ VDD ≤ 5.5V		20		38		ns
		1.8V ≤VDD ≤ 5.5V		28		55		ns
SDIp hold time (from CLKp↑)	tKSI1	1.8V ≤VDD ≤ 5.5V		5		10		ns

SCLKp↓→SDOp Delay time	tKSO1	1.8V ≤VDD ≤ 5.5V C = 20pF Note1		5		10	ns

Note 1. C is the load capacitance of the SCLKp and SDOp output lines.

Caution: Select the normal input buffer for the SDIp pin and the normal output mode for the SDOp pin and SCLKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

3) 3-wire serial I/O(SSPI)(slave mode, external clock input)

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

Parameter	Symbol	Conditions		–40 ～ +85℃		+85 ～ +105℃		Unit
				MIN	MAX	MIN	MAX	
SCLKp cycle time	tKCY2	4.0V ≤ VDD ≤ 5.5V	20MHz < fMCK	8/fMCK		16/fMCK		ns
			fMCK ≤20MHz	6/fMCK		12/fMCK		ns
		2.7V ≤ VDD ≤ 5.5V	16MHz < fMCK	8/fMCK		16/fMCK		ns
			fMCK ≤16MHz	6/fMCK		12/fMCK		ns
		2.4V ≤ VDD ≤ 5.5V		6/fMCK and 500		12/fMCK and 1000		ns
		1.8V ≤VDD ≤ 5.5V		6/fMCK and 750		12/fMCK and 1500		ns
SCLKp high-/low-level width	tKH2, tKL2	4.0V ≤ VDD ≤ 5.5V		tKCY1/2–7		tKCY1/2–14		ns
		2.7V ≤ VDD ≤ 5.5V		tKCY1/2–8		tKCY1/2–16		ns
		1.8V ≤VDD ≤ 5.5V		tKCY1/2–18		tKCY1/2–36		ns
SDIp setup time (to SCLKp↑)	tSIK2	2.7V ≤ VDD ≤ 5.5V		1/fMCK+20		1/fMCK+40		ns
		1.8V ≤VDD ≤ 5.5V		1/fMCK+30		1/fMCK+60		ns
SDIp hold time (from SCLKp↑)	tKSI2	1.8V ≤VDD ≤ 5.5V		1/fMCK+31		1/fMCK+62		ns
SCLKp↓→SDOp Delay time	tKSO2	2.7V ≤ VDD ≤ 5.5V C=30pF note1			2/fMCK +44		2/fMCK +66	ns
		2.4V ≤ VDD ≤ 5.5V C=30pF note1			2/fMCK +75		2/fMCK +113	ns
		1.8V ≤VDD ≤ 5.5V C=30pF note1			2/fMCK +100		2/fMCK +150	ns

Note 1. C is the load capacitance of the SCLKp and SDOp output lines.

Caution: Select the normal input buffer for the SDIp pin and the normal output mode for the SDOp pin and SCLKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

4) 4-wire serial I/O(SPI) (slave mode, external clock input)

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

Parameter	Symbol	Conditions		–40 ～ +85℃		+85 ～ +105℃		Unit
				MIN	MAX	MIN	MAX	
SSI00 setup time	tSSIK	DAPmn=0	2.7V ≤ VDD ≤ 5.5V	120		240		ns
			1.8V ≤VDD ≤ 5.5V	200		400		ns
		DAPmn=1	2.7V ≤ VDD ≤ 5.5V	1/fMCK+120		1/fMCK+240		ns
			1.8V ≤VDD ≤ 5.5V	1/fMCK+200		1/fMCK+400		ns
SSI00 hold time	tKSSI	DAPmn=0	2.7V ≤ VDD ≤ 5.5V	1/fMCK+120		1/fMCK+240		ns
			1.8V ≤VDD ≤ 5.5V	1/fMCK+200		1/fMCK+400		ns
		DAPmn=1	2.7V ≤ VDD ≤ 5.5V	120		240		ns
			1.8V ≤VDD ≤ 5.5V	200		400		ns

Caution: Select the normal input buffer for the SDIp pin and the normal output mode for the SDOp pin and SCLKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

5) simplified I²C mode

（TA=–40～+105℃, 2.0V≤EVDD=VDD≤5.5V, VSS=EVSS=0V）

Parameter	Symbol	Conditions	–40 ～ +85℃		+85 ～ +105℃		Unit
			MIN	MAX	MIN	MAX	
SCLr clock frequency	fSCL	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ		1000note1		400note1	KHz
		1.8V ≤EVDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ		400note1		100note1	KHz
		1.8V ≤EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ		300note1		75note1	KHz
Hold time when SCLr = “L”	tLOW	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	475		1200		ns
		1.8V ≤EVDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1150		4600		ns
		1.8V ≤EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1550		6500		ns
Hold time when SCLr = “H”	tHIGH	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	475		1200		ns
		1.8V ≤EVDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1150		4600		ns
		1.8V ≤EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1550		6500		ns
Data setup time (reception)	tSU:DAT	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK+85 note2		1/fMCK+ 220note2		ns
		1.8V ≤EVDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ	1/fMCK+145 note2		1/fMCK+ 580note2		ns
		1.8V ≤EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ	1/fMCK+230 note2		1/fMCK+ 1200note2		ns
Data hold time (transmission)	tHD:DAT	2.7V ≤ EVDD ≤ 5.5V Cb = 50 pF, Rb = 2.7 kΩ		305		770	ns
		1.8V ≤EVDD ≤ 5.5V Cb = 100 pF, Rb = 3 kΩ		355		1420	ns
		1.8V ≤EVDD ≤ 2.7V Cb = 100 pF, Rb = 5 kΩ		405		2070	ns

Note:

1. The value must also be equal to or less than fMCK/4.
2. Set the fMCK value to keep the hold time of SCLr = “L” and SCLr = “H”.

6.7.2 Serial Interface IICA

1) I²C standard mode

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

Parameter	Symbol	Conditions	Spec		Unit
			MIN	MAX	
SCLA0 clock frequency	fSCL	Standard mode: fCLK≥1MHz		100	KHz
Setup time of restart condition	tSU:STA		4.7		us
Hold time Note 1	tHD:STA		4.0		us
Hold time when SCLA0 = “L”	tLOW		4.7		us
Hold time when SCLA0 = “H”	tHIGH		4.0		us
Data setup time (reception)	tSU:DAT		250		ns
Data hold time (transmission) Note 2	tHD:DAT		0	3.45	us
Setup time of stop condition	tSU:STO		4.0		us
Bus-free time	tBUF		4.7		us

Note:

1. The first clock pulse is generated after this period when the start/restart condition is detected.
2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark:

The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb=400pF, Rb=2.7kΩ

2) I²C fast mode

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

Parameter	Symbol	Conditions	Spec		Unit
			MIN	MAX	
SCLA0 clock frequency	fSCL	Fast mode: fCLK≥3.5MHz		400	KHz
Setup time of restart condition	tSU:STA		0.6		us
Hold time Note 1	tHD:STA		0.6		us
Hold time when SCLA0 = “L”	tLOW		1.3		us
Hold time when SCLA0 = “H”	tHIGH		0.6		us
Data setup time (reception)	tSU:DAT		100		ns
Data hold time (transmission) Note 2	tHD:DAT		0	0.9	us
Setup time of stop condition	tSU:STO		0.6		us
Bus-free time	tBUF		1.3		us

Note:

1. The first clock pulse is generated after this period when the start/restart condition is detected.
2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark:

The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode:Cb=320pF, Rb=1.1kΩ

3) I²C fast mode plus

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

Parameter	Symbol	Conditions	Spec		Unit
			MIN	MAX	
SCLA0 clock frequency	fSCL	Fast mode plus: fCLK≥10MHz		1000	KHz
Setup time of restart condition	tSU:STA		0.26		us
Hold time Note 1	tHD:STA		0.26		us
Hold time when SCLA0 = “L”	tLOW		0.5		us
Hold time when SCLA0 = “H”	tHIGH		0.26		us
Data setup time (reception)	tSU:DAT		50		ns
Data hold time (transmission) Note 2	tHD:DAT		0	0.45	us
Setup time of stop condition	tSU:STO		0.26		us
Bus-free time	tBUF		0.5		us

Note:

1. The first clock pulse is generated after this period when the start/restart condition is detected.
2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark:

The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus:Cb=120pF, Rb=1.1kΩ

6.8 Analog Characteristics

6.8.1 A/D Converter Characteristics

Classification of A/D converter characteristics

Input channel \ Reference Voltage	Reference voltage(+)=AV_{REFP} Reference voltage(–)=AV_{REFM}	Reference voltage(+)=V_{DD} Reference voltage(–)=V_{SS}
ANI0～ANI36	Refer to 6.8.1 (1)	Refer to 6.8.1(2)
Internal reference voltageTemperature sensor output voltage		

1) When reference voltage (+)=AVREFP/ANI0, reference voltage (–)=AVREFM/ANI1

(TA=-40～+105℃, 1.8V≤AVREFP≤VDD≤5.5V, VSS=0V, reference voltage(+)=AVREFP, reference voltage(–)=AVREFM=0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				12		bit
Overall error Note 1	ET	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V		3		LSB
Zero-scale error Note 1	E_{ZS}	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V		0		LSB
Full-scale error Note 1	E_{FS}	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V		0		LSB
Integral linearity error Note 1	EL	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V	-1		1	LSB
Differential linearity error Note 1	ED	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V	-1.5		1.5	LSB
Conversion time Note3	t_{CONV}	12-bit resolution Target pin:ANI2～ANI36	1.8V≤VDD≤5.5V	45			1/fadc
		12-bit resolution Target pin:Internal reference voltage,and temperature sensor output voltage, PGAoutput voltage	1.8V≤VDD≤5.5V	72			1/fadc
External input resistance	R_{AIN}	R_{AIN} < (Ts / (fad x Cadc x ln(2^{12+2})) - R_{ADC})			7.5 Note4		kΩ
Sampling switch resistance	R_{ADC}					1.5	kΩ
Sample and hold capacitance	C_{ADC}				2		pF
Analog input voltage	V_{AIN}	ANI2～ANI36		0		AV_{REFP}	V
		Internal reference voltage (1.8V≤VDD≤5.5V)		V_{BGR} Note2			V
		Temperature sensor output voltage (1.8V≤VDD≤5.5V)		V_{TMPS} Note2			V

Note:

1) Excludes quantization error (±1/2 LSB).
2) Refer to “6.8.2 Temperature sensor characteristics/internal reference voltage characteristic”.
3) Tmclk is the operating clock cycle of AD, and the maximum operating frequency is 48MHz.
4) Guaranteed by design, mass production without testing. The typical value is the default sampling period TS = 13.5, and the conversion speed is the calculated value under the condition of fad = 64 MHz.

2) When reference voltage (+) =VDD, reference voltage (–) =VSS
(TA=–40～ +105℃, 1.8V≤ EVDD= VDD≤ 5.5V, VSS=EVSS=0V, reference voltage (+)=VDD, reference voltage (–)=VSS)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				12		bit
Overall error Note 1	ET	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V		6		LSB
Zero-scale error Note 1	E_{ZS}	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V		0		LSB
Full-scale error Note 1	E_{FS}	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V		0		LSB
Integral linearity error Note 1	EL	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V	-2		2	LSB
Differential linearity error Note 1	ED	12-bit resolution	1.8V ≤AV_{REFP} ≤5.5V	-3		3	LSB
Conversion time Note3	t_{CONV}	12-bit resolution Target pin:ANI2～ANI36	1.8V≤VDD≤5.5V	45			1/fadc
		12-bit resolution Target pin:Internal reference voltage,and temperature sensor output voltage, PGAoutput voltage	1.8V≤VDD≤5.5V	72			1/fadc
External input resistance	R_{AIN}	R_{AIN} < (Ts / (fad x Cadc x ln(2^{12+2})) - R_{ADC})			7.5 Note4		kΩ
Sampling switch resistance	R_{ADC}					1.5	kΩ
Sample and hold capacitance	C_{ADC}				2		pF
Analog input voltage	V_{AIN}	ANI0～ANI36		0		V_{DD}	V
		Internal reference voltage (1.8V≤VDD≤5.5V)		V_{BGR} Note2			V
		Temperature sensor output voltage (1.8V≤VDD≤5.5V)		V_{TMPS} Note2			V

Note:

1) Excludes quantization error (±1/2 LSB).
2) Refer to “6.8.2 Temperature sensor characteristics/internal reference voltage characteristic”.
3) Tmclk is the operating clock cycle of AD, and the maximum operating frequency is 64MHz.
4) Guaranteed by design, mass production without testing. The typical value is the default sampling period TS = 13.5, and the conversion speed is the calculated value under the condition of fad = 64 MHz.

6.8.2 Temperature Sensor Characteristics/Internal Reference Voltage Characteristic

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Temperature sensor output voltage	VTMPS25	ADS = 80H, TA=+25℃		1.09		V
Internal reference voltage	VBGR	TA=-40 ~10℃	1.25Note1	1.45	1.65Note1	V
		TA=10 ~70℃	1.38Note1	1.45	1.50Note1	V
		TA=70 ~105℃	1.30Note1	1.45	1.60Note1	V
Temperature coefficient	FVTMPS			-3.5		mV/℃
Operation stabilization wait time	tAMP		5			us

Note:

1.The low temperature specification value is guaranteed by the design, and the low temperature condition is not measured for mass production.

6.8.3 Comparator

(TA=–40～+105℃, 1.8V≤VDD≤5.5V, VSS=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input offset voltage	V_{IOCMP}				±10	±40	mV
Input voltage range	Ivcmp			0		VDD	V
Internal reference voltage deviation	ΔV_{IREF}	CmRVM register value : 7FH ~ 80H (m = 0, 1)				±2	LSB
		Other than above				±1	LSB
Response Time	tCR,tCF	Input amplitude±100mV			70	150	ns
Operation stabilization Time Note 1	tCMP	CMPn=0->1	VDD= 3.3 ~ 5.5V			1	us
			VDD= 1.8 ~ 3.3V			3	
Reference voltage stabilization wait time	tVR	CVRE=0->1 Note2				20	us
Operation current	I_{CMPDD}	Separately, it is defined as the operation current of peripheral functions.					

Note1: Time taken until the comparator satisfies the DC/AC characteristics after the comparator operation enable signal is switched (CMPnEN = 0 → 1).

Note2: Enable comparator output (CnOE bit = 1; n = 0 to 1) after enabling operation of the internal reference voltage generator

(by setting the CVREm bit to 1; m = 0 to 1) and waiting for the operation stabilization time to elapse.

6.8.4 PGA

(T_A=–40～+105℃, 1.8V≤VDD≤5.5V, V_{SS}=0V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input offset voltage	V_{IOPGA}				±3	±10	mV
Input voltage range	V_{IPGA}			0		0.9xVDD/ Gain	V
Output voltage range	V_{IOHPGA}			0.93xVDD			V
	V_{IOLPGA}					0.07xVDD	V
Gain error		x4				±1	%
		x8				±1	%
		x10				±1	%
		x12				±2	%
		x14				±2	%
		x16				±2	%
		x32				±3	%
Slew rate	SR_{RPGA}	Rising Vin= 0.1VDD/gain to 0.9VDD/gain. 10 to 90% of output voltage amplitude	4.0 V ≤ VDD ≤ 5.5 V (Other than x32)	3.5			V/us
			4.0 V ≤ VDD ≤ 5.5 V (x32)	3.0			
			2.0 V ≤ VDD ≤ 4.0V	0.5			
	SR_{FPGA}	Falling Vin= 0.1VDD/gain to 0.9VDD/gain. 90 to 10% of output voltage amplitude	4.0 V ≤ VDD ≤ 5.5 V (Other than x32)	3.5			
			4.0 V ≤ VDD ≤ 5.5 V (x32)	3.0			
			2.0 V ≤ VDD ≤ 4.0V	0.5			
Reference voltage stabilization wait time Note 1	t_{PGA}	x4				5	us
		x8				5	us
		x10				5	us
		x12				10	us
		x14				10	us
		x16				10	us
		x32				10	us
Operation current	I_{PGADD}	Separately, it is defined as the operation current of peripheral functions.					

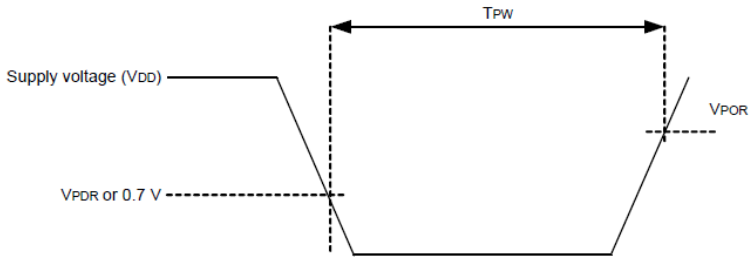
Note1.Time required until a state is entered where the DC and AC specifications of the PGA are satisfied after the PGA operation has been enabled (PGAEN = 1).

6.8.5 POR Circuit Characteristics

(T_A=–40～+105°C, V_{SS}=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Power on/down reset threshold	VPOR	Voltage threshold on VDD rising		1.50	1.75	V
	VPDR	Voltage threshold on VDD falling	1.37	1.45		V
Minimum pulse width Note 1	TPW		300			us

Note1. Minimum time required for a POR reset when VDD exceeds below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



6.8.6 LVD Circuit Characteristics

1) Reset Mode and Interrupt Mode

(T_A=–40～+105℃, $V_{PDR} \leqslant V_{DD} \leqslant$5.5V, V_{SS}=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Voltage detection threshold	VLVD0	Rising edge		4.06	4.14	V
		Falling edge	3.78	3.98		V
	VLVD1	Rising edge		3.75		V
		Falling edge		3.67		V
	VLVD2	Rising edge		3.13		V
		Falling edge		3.06		V
	VLVD3	Rising edge		3.02		V
		Falling edge		2.96		V
	VLVD4	Rising edge		2.92		V
		Falling edge		2.86		V
	VLVD5	Rising edge		2.81		V
		Falling edge		2.75		V
	VLVD6	Rising edge		2.71		V
		Falling edge		2.65		V
	VLVD7	Rising edge		2.61		V
		Falling edge		2.55		V
	VLVD8	Rising edge		2.50		V
		Falling edge		2.45		V
	VLVD9	Rising edge		2.09		V
		Falling edge		2.04		V
	VLVD10	Rising edge		1.98		V
		Falling edge		1.94		V
	VLVD11	Rising edge		1.88	1.91	V
		Falling edge	1.80	1.84		V
Minimum pulse width	tLW		300			us
Detection delay time					300	us

2) Interrupt & Reset Mode

(T_A=–40～+105℃, V_{PDR} ≤V_{DD}≤5.5V, V_{SS}=0V)

Parameter	Symbol	Conditions			MIN	TYP	MAX	Unit
Voltage detection threshold	V_{LVDA0}	V_{POC2}, V_{POC1}, V_{POC0}=0, 0, 0,falling reset voltage			1.60	1.63		V
	V_{LVDA1}	LVIS1, LVIS0=1, 0		Rising release reset voltage		1.77	1.81	V
				Falling interrupt voltage	1.70	1.73		V
	V_{LVDA2}	LVIS1, LVIS0=0, 1		Rising release reset voltage		1.88		V
				Falling interrupt voltage		1.84		V
	V_{LVDA3}	LVIS1, LVIS0=0, 0		Rising release reset voltage		2.92		V
				Falling interrupt voltage		2.86		V
	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0}=0, 0, 1,falling reset voltage				1.84		V
	V_{LVDB1}	LVIS1, LVIS0=1, 0		Rising release reset voltage		1.98		V
				Falling interrupt voltage		1.94		V
	V_{LVDB2}	LVIS1, LVIS0=0, 1		Rising release reset voltage		2.09		V
				Falling interrupt voltage		2.04		V
	V_{LVDB3}	LVIS1, LVIS0=0, 0		Rising release reset voltage		3.13		V
				Falling interrupt voltage		3.06		V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0}=0, 1, 0,falling reset voltage				2.45		V
	V_{LVDC1}	LVIS1, LVIS0=1, 0		Rising release reset voltage		2.61		V
				Falling interrupt voltage		2.55		V
	V_{LVDC2}	LVIS1, LVIS0=0, 1		Rising release reset voltage		2.71		V
				Falling interrupt voltage		2.65		V
	V_{LVDC3}	LVIS1, LVIS0=0, 0		Rising release reset voltage		3.75		V
				Falling interrupt voltage		3.67		V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0}=0, 1, 1,falling reset voltage				2.75		V
	V_{LVDD1}	LVIS1, LVIS0=1, 0		Rising release reset voltage		2.92		V
				Falling interrupt voltage		2.86		V
	V_{LVDD2}	LVIS1, LVIS0=0, 1		Rising release reset voltage		3.02		V
				Falling interrupt voltage		2.96		V
	V_{LVDD3}	LVIS1, LVIS0=0, 0		Rising release reset voltage		4.06	4.14	V
				Falling interrupt voltage	3.90	3.98		V

6.8.7 Reset Time and Power Supply Voltage Rising Slope Characteristics

(T_A=–40～+105°C, V_{SS}=0V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Reset time	T_{RESET}			1		Ms
Power supply voltage rising slope	SVDD				54	V/ms

6.9 Memory Characteristics

6.9.1 Flash Memory

(TA=–40～+105˚C, 1.8V≤VDD≤5.5V, VSS=0V)

Symbol	Parameter	Conditions	MIN	MAX	Unit
Tprog	Word Program(32bit)	Ta=–40～+105˚C	24	30	us
Terase	Sector erase(512B)	Ta=–40～+105˚C	4	5	ms
	Chip erase	Ta=–40～+105˚C	20	40	ms
N_{END}	Endurance	Ta=–40～+105˚C	100		kcycle
t_{RET}	Data retention	100 kcycle(2) at Ta = 105˚C	20		Years

Note1: Data based on characterization results, not tested in production.

Note2: Cycling performed over the whole temperature range.

6.9.2 RAM Memory

(TA=–40～+105˚C, 1.8V≤VDD≤5.5V, VSS=0V)

Symbol	Parameter	Conditions	MIN	MAX	Unit
Vramhold	RAM Hold Voltage	Ta=–40～+105˚C	0.8		V

6.10 Electrical Sensitivity Characteristics

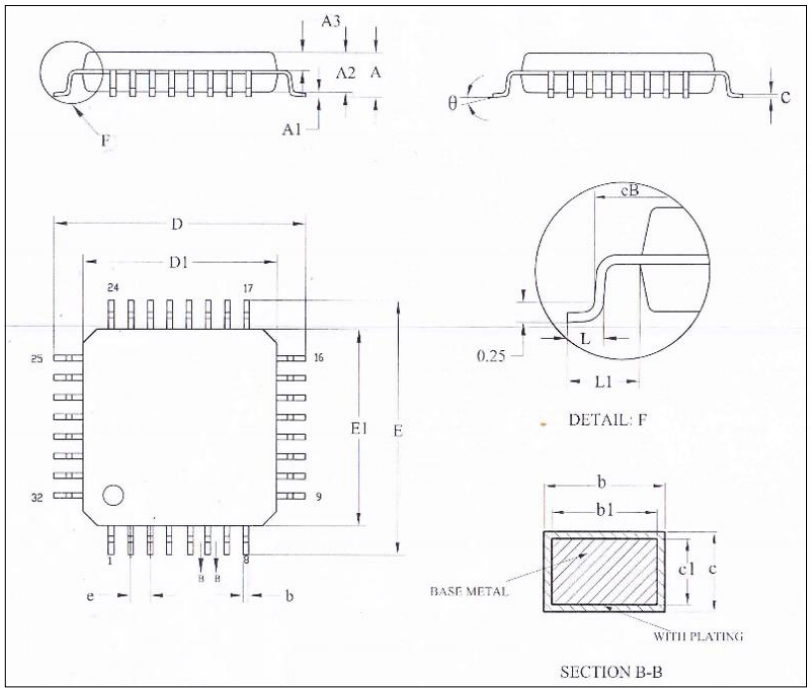
6.10.1 Electrostatic Discharge (ESD)

Symbol	Parameter	Conditions	Class
VESD(HBM)	Electrostatic discharge voltage (human body model)	TA = +25℃, conforming to JESD22-A114	3A

Note: Data based on characterization results, not tested in production.

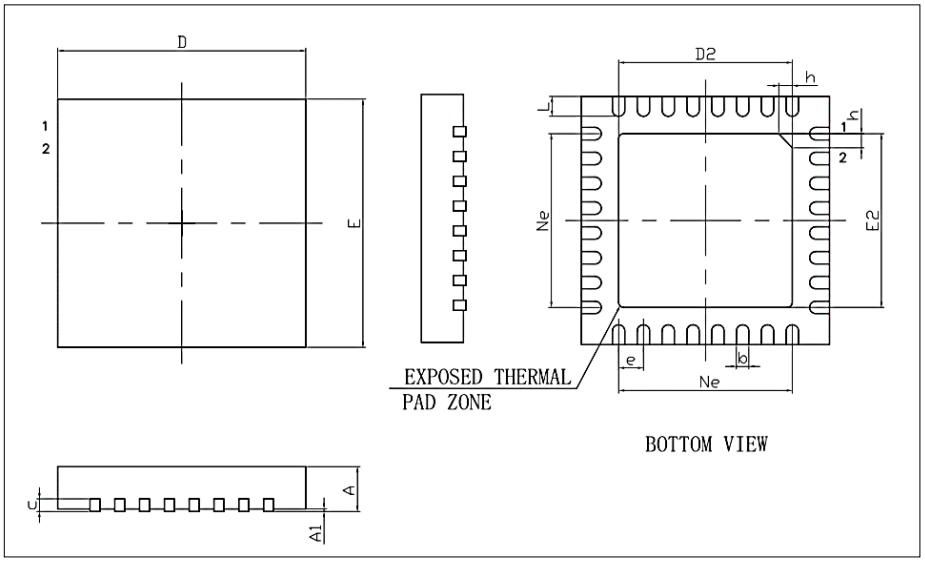
7 Package Drawings

7.1 LQFP32 (7x7mm, 0.8mm)



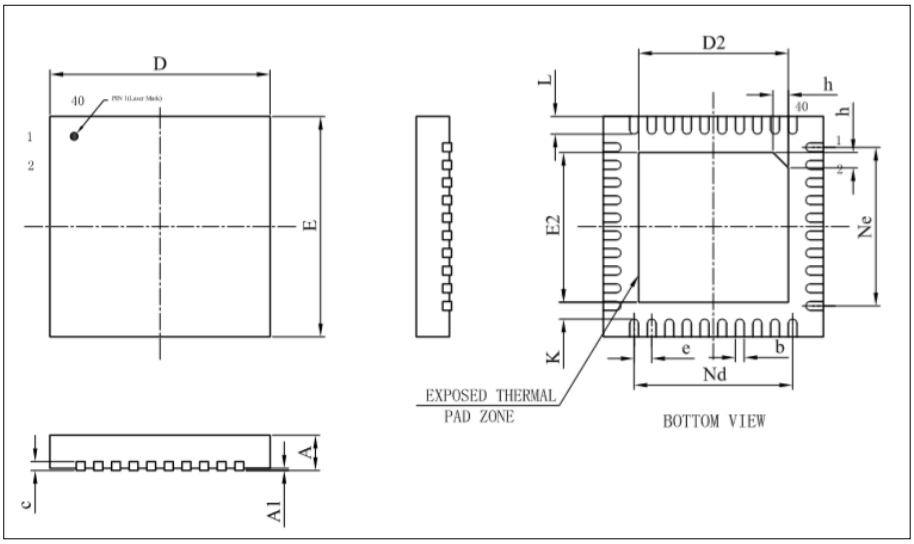
Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.33	-	0.41
b1	0.32	0.35	0.38
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.80BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

7.2 QFN32（5x5mm，0.5mm）



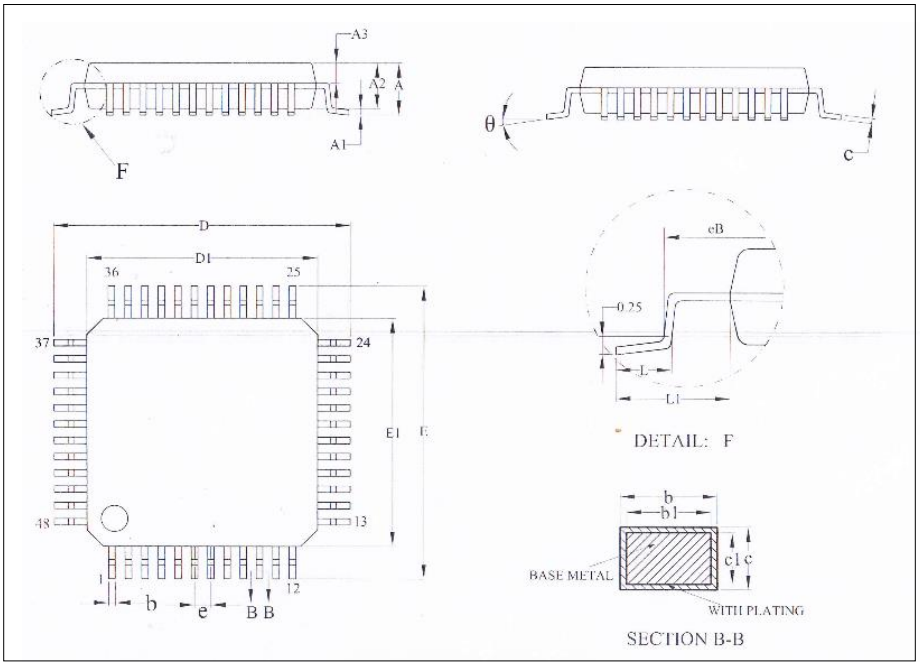
Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

7.3 QFN40 (5x5mm, 0.4mm)



Symbol	Millimeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.30	3.40	3.50
e	0.40BSC		
Nd	3.60BSC		
E	4.90	5.00	5.10
E2	3.30	3.40	3.50
Ne	3.60BSC		
L	0.35	0.40	0.45
K	0.20	-	-
h	0.30	0.35	0.40

7.4 LQFP48 (7x7mm, 0.5mm)



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.25
e	0.50BSC		
L	0.45	-	0.75
L1	1.00REF		
θ	0°	-	7°

8 Revision History

Rev.	Date	Description
V1.00	2020.12.30	First Version Issue
V1.40	2023.2.20	1) 6.9, 6.10: Added subsections of 6.9, 6.10 characteristic descriptions. 2) 6.4.2, 6.8.2: Added notes on parameters for low temperature conditions. 3) 1.2, 1.3, 7.1: Added product descriptions for QFN32 package. 4) 4.1, 4.3: Added port type descriptions. 5) 6.8: Modified some specification values for analogue characteristics. 6) Full text: Uniformed the format.
V1.4.1	Aug 2023	1) Modified 1.1 Introduction 2) Adjusted the format of the pinout diagram
V1.4.2	Jan 2024	1) Modify the contents of section 6.1 / 6.4.1 2) Corrected the number of Timer4 multiple PWM in section 5.13.2 3) Corrected the cover page