# BAT32G157 datasheet

## ARM® Cortex®-M0+ based, ultra low power consumption 32-bit microcontroller

## Built-in 256K byte Flash, rich simulation function, timer and various communication interfaces

## Rev 2.01

# Features:

- **Ultra-low power consumption operating environment:**
  - Power supply voltage range: 1.8V to 5.5V
  - Temperature range: -40℃ to 105℃
  - Low power consumption mode: sleep mode, deep sleep mode
  - Operating power consumption: 120uA/MHz@64MHz
  - Power consumption in deep sleep mode: 0.7uA
  - Deep sleep mode+32.768K+RTC：1.2uA
- **Core:**
  - ARM®32-bitCortex®-M0+ CPU
  - Working frequency：32KHz～64MHz
- **Memory:**
  - 256KB Flash memory, with program and data storage shared
  - 2.5KB dedicated data Flash memory
  - 32KB SRAM memory with parity check
  - Support Remap function, you can choose to boot from Boot area, Code Flash area or RAM area
- **Power and reset management:**
  - Built-in power-on reset (POR) circuit
  - Built-in voltage detection (LVD) circuit (threshold voltage can be set)
- **Clock management:**
  - Built-in high-speed vibrator, accuracy (±1%). Can provide 1MHz～64MHz system clock and peripheral module operation clock
  - Built-in 15KHz low-speed oscillator
  - Built-in 2 PLL
  - Support 1MHz～20MHz external crystal oscillator
  - Support 32.768KHz external crystal oscillator
- **Multiplier/divider module:**
  - Multiplier：Support single cycle 32bit multiplication operation
  - Divider：Support 32bit signed integer division operation, only 8 CPU clock cycles to complete an operation
- **Enhanced DMA controller:**
  - Interrupt trigger start.
  - Transmission mode is selectable (normal transmission mode, repeated transmission mode, block transmission mode and chain transmission mode)
  - The transmission source/destination area is optional for the full address space range
- **Linkage controller:**
  - The event signals can be linked together to realize the linkage of peripheral functions.
  - 15 types of event input, 4 types of event trigger.
- **Abundant analog peripheral:**
  - 12-bit precision ADC converter, conversion rate 1.42Msps, 35 external analog channels, internal optional PGA0 output as conversion channel, with temperature sensor, support single-channel conversion mode and multi-channel scan conversion mode Conversion range: 0 to positive reference voltage
  - Comparator (CMP), built-in two-channel comparator with hysteresis, optional input source, reference voltage can be external reference voltage or internal reference voltage
  - Programmable gain amplifier (PGA), built-in one channel PGA, can set 1/2/4/8/16/32/64/128 times gain, with external GND pin (can be used as differential mode), output with sample and hold Circuit to support offset voltage trimming
- **Input/output port:**
  - Number of I/O port：44～58
  - Can switch between N-channel open drain and internal pull-up and pull-down
  - Built-in button interrupt detection function
  - Built-in clock output/buzzer output control circuit
- **Serial two-wire debugger (SWD)**
- **Abundant timer:**
  - 16-bit timer: 12 channels
  - 15-bit interval timer: 1
  - Real-time clock (RTC): 1 (with perpetual calendar, alarm clock function, and supports a wide range of clock correction)
  - Watchdog timer（WWDT）:1
  - SysTick timer
- **Abundant and flexible interface：**
  - 3-channel serial communication unit: each channel can be freely configured as a 1-channel standard UART, 2-channel SPI or 2-channel simple I2C
  - Standard SPI：2 channel（support 8bit and16bit）
  - Standard I2C：2 channel
  - SSIE：1 channel

- **USB port：**
  - Compatible with USB 2.0 specification
  - Can be used as host controller or device controller
  - Support USB 2.0 full-speed and low-speed transmission
  - Support synchronous transmission, control transmission, batch transmission and interrupt transmission
  - Compatible with USB BC1.2
  - On-The-Go（OTG） feature
- **security function:**
  - Comply with relevant standards of IEC/UL 60730
  - Abnormal storage space access error
  - Support RAM parity check
  - Support hardware CRC check
  - Support important SFR protection to prevent misoperation
  - 128-bit unique ID number
  - Flash secondary protection in debug mode (level1: only the entire flash area can be erased, not read or write; level2: the emulator connection is invalid, and the flash operation is not possible)
- **Encapsulation:** Support multiple encapsulation of 48 Pin and 64 Pin

# 1 Overview

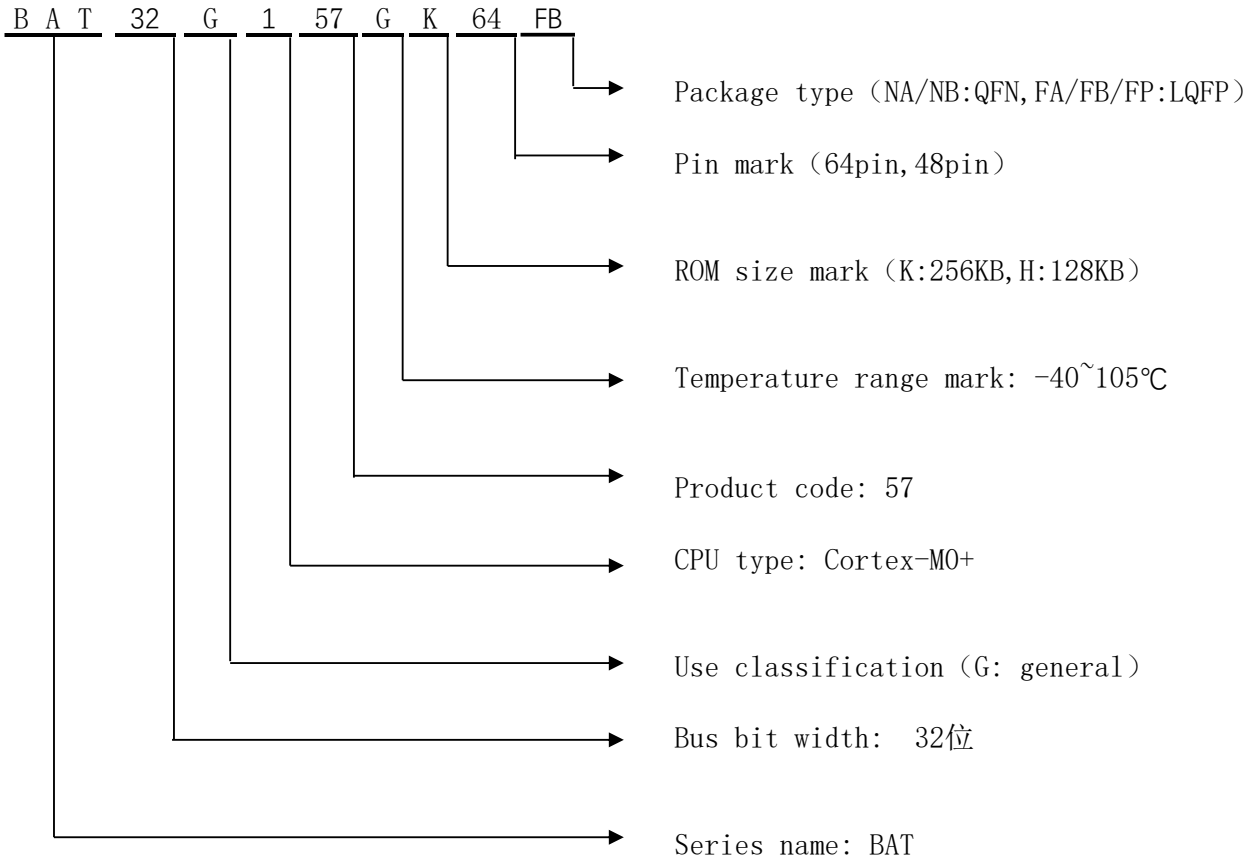
## 1.1 Introduction

Ultra-low power consumption BAT32G157 uses high-performance 32-bit RISC core of ARM®Cortex®-M0+, can work at a frequency of up to 64 MHz, and adopts high-speed embedded flash memory (SRAM max. 32KB, program/data flash memory max. 256KB ). This product integrates multiple standard interfaces of I2C, SPI, UART, LIN, USB, and SSIE. Integrated 12bit A/D converter, temperature sensor, comparator, programmable gain amplifier. Among them, the 12bit A/D converter can collect external sensor signals, reducing system design costs. The temperature sensor integrated in the chip can realize real-time monitoring of the external ambient temperature. The internally integrated comparator of the chip can support both high-speed and low-speed operating modes. In the high-speed mode, it can support the control feedback of the high-speed motor, and in the low-speed mode, it can be used for battery monitoring. Integrated 12-channel 16bit timer module, and equipped with EPWM control circuit, combined with the timer can realize the control of one DC motor or two stepper motors.

BAT32G157 also has excellent low-power performance, supports two low-power modes of sleep and deep sleep, and is designed to be flexible. Its operating power consumption is 120uA/MHz@64MHz, and the power consumption is only 0.7uA in deep sleep mode, which is suitable for battery-powered low-power devices. At the same time, due to the integrated event linkage controller, direct connection between hardware modules can be realized without the intervention of the CPU, which is faster than using interrupt response, while reducing the frequency of CPU activity and prolonging the battery life.

These features make the BAT32G157 microcontroller series can be widely used in consumer civil products, such as household appliances, mobile devices, etc.

## 1.2 Product model list




List of products of BAT32G157:

| Number of Pin | Encapsulation | Product model |
|---|---|---|
| 48 pin | 48-pin plastic package LQFP (7×7mm, 0.5mm pitch) | BAT32G157GK48FA |
| | 48-pin plastic package QFN (6×6mm, 0.4mm pitch) | BAT32G157GK48NB |
| 64 pin | 64-pin plastic package LQFP (7×7mm, 0.4mm pitch) | BAT32G157GK64FB |

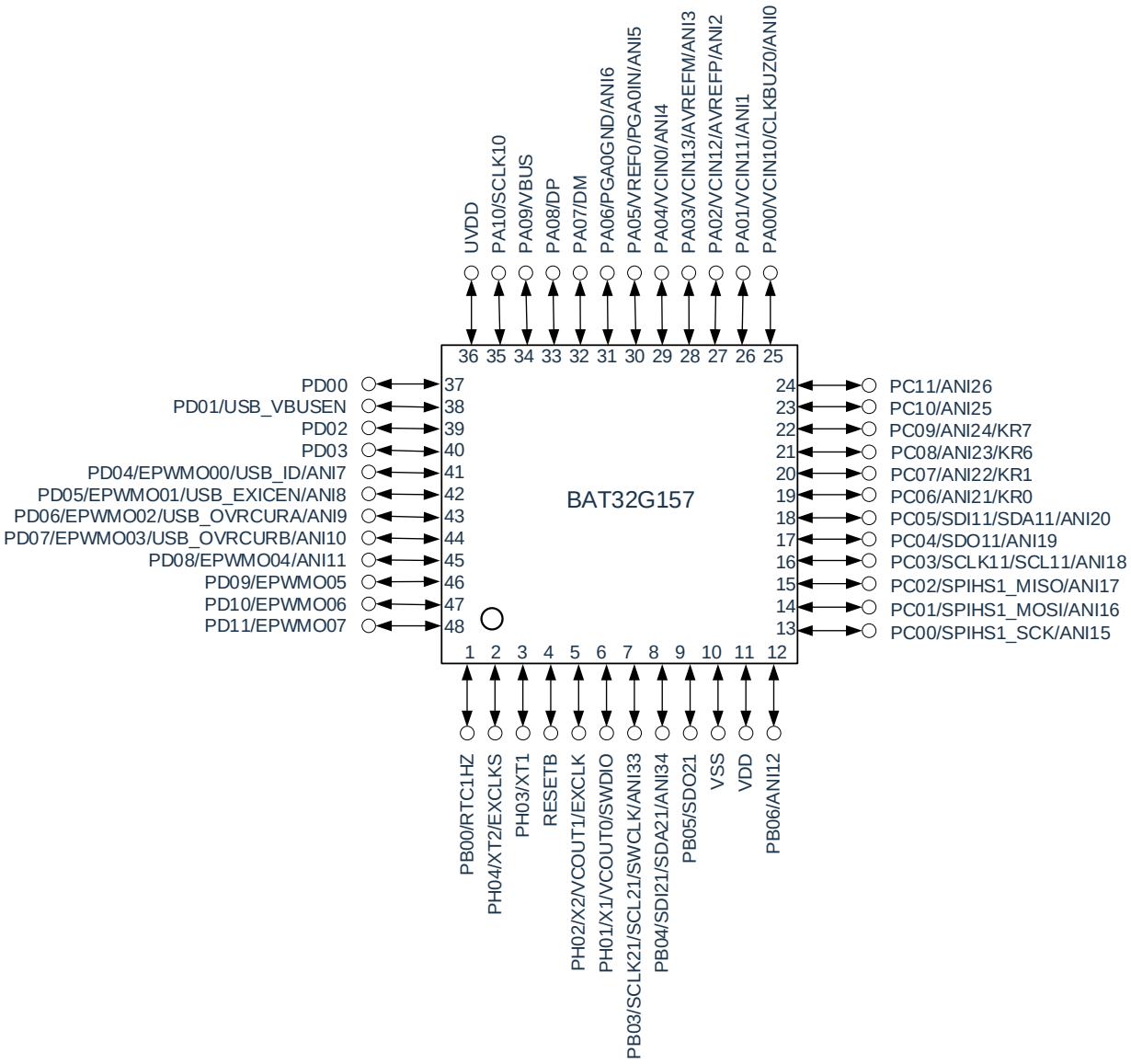
FLASH、SRAM capacity:

| Flash memory | Special data Flash memory | SRAM | BAT32G157 | |
|---|---|---|---|---|
| | | | 48 pin | 64 pin |
| 256KB | 2.5KB | 32KB | BAT32G157GK48FA<br>BAT32G157GK48NB | BAT32G157GK64FB |

## 1.3 Pin connection diagram（Top View）

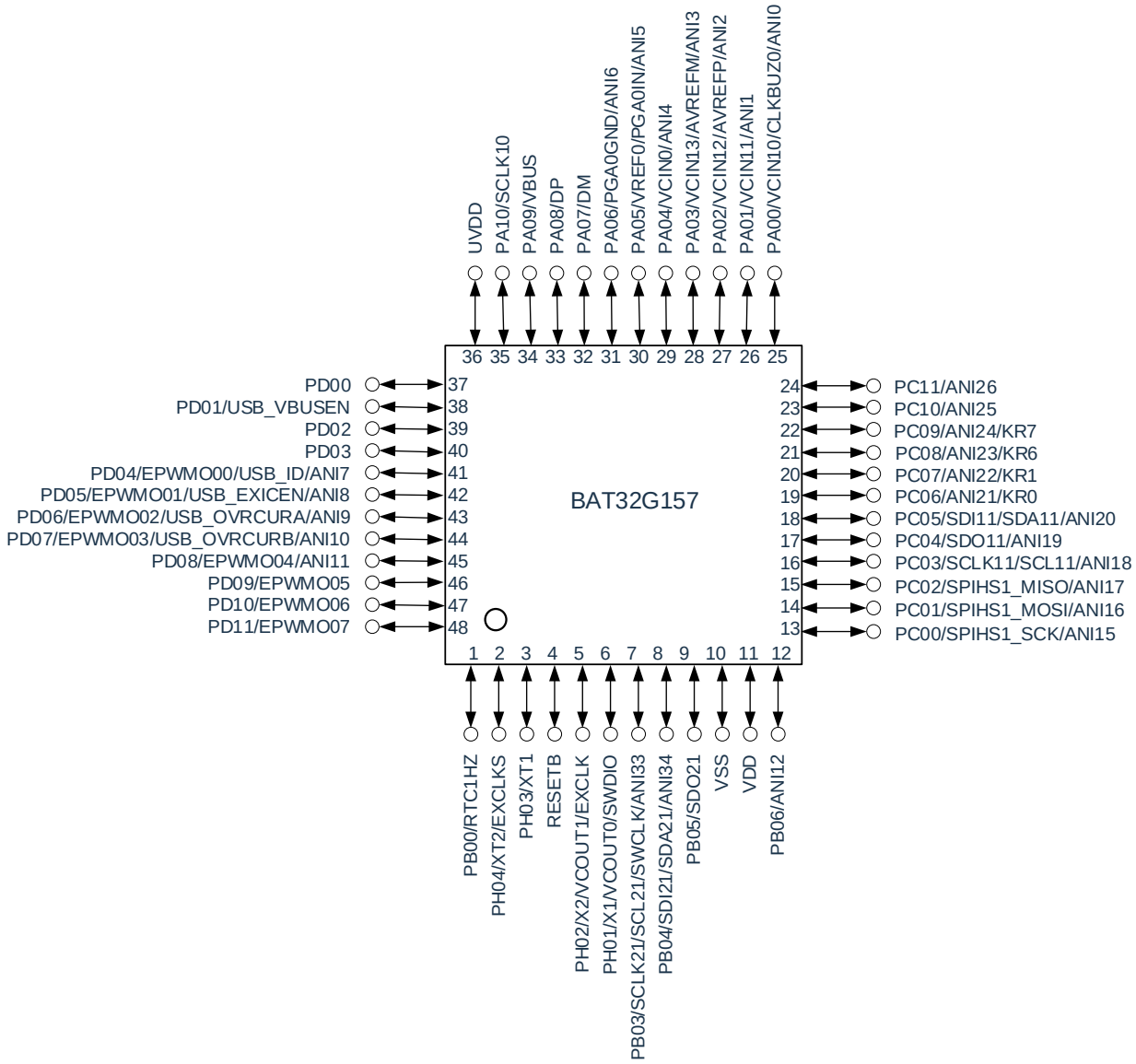
### 1.3.1 48 pin product – LQFP48

- 48-pin plastic package LQFP (7×7mm, 0.5mm pitch)



## 1.3.2 48 pin product – QFN48

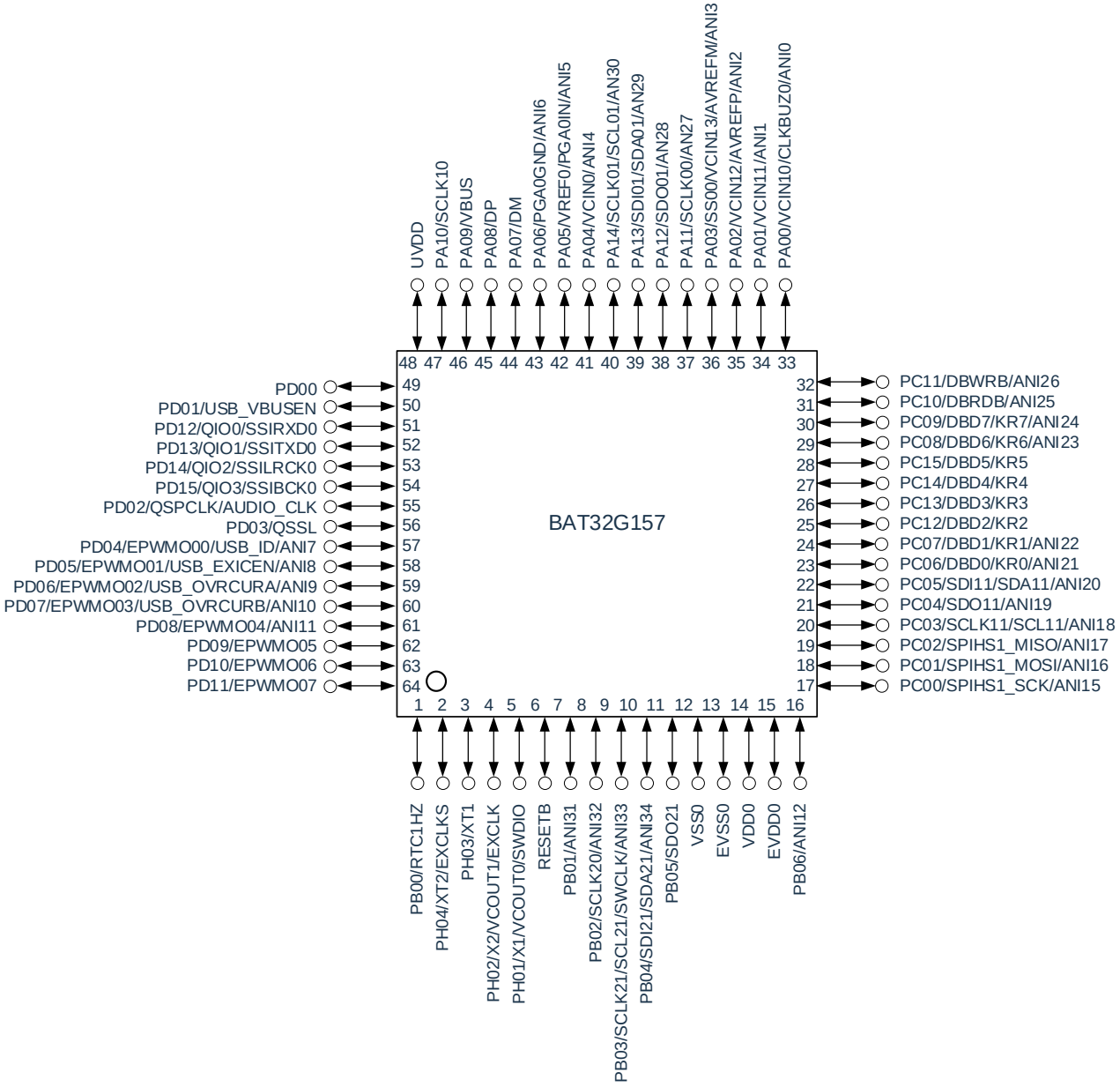
- 48-pin plastic package QFN48 ((6×6mm, 0.4mm pitch))




Note: The unmarked digital function support pins in the figure are configurable, see section 4.1 for details.

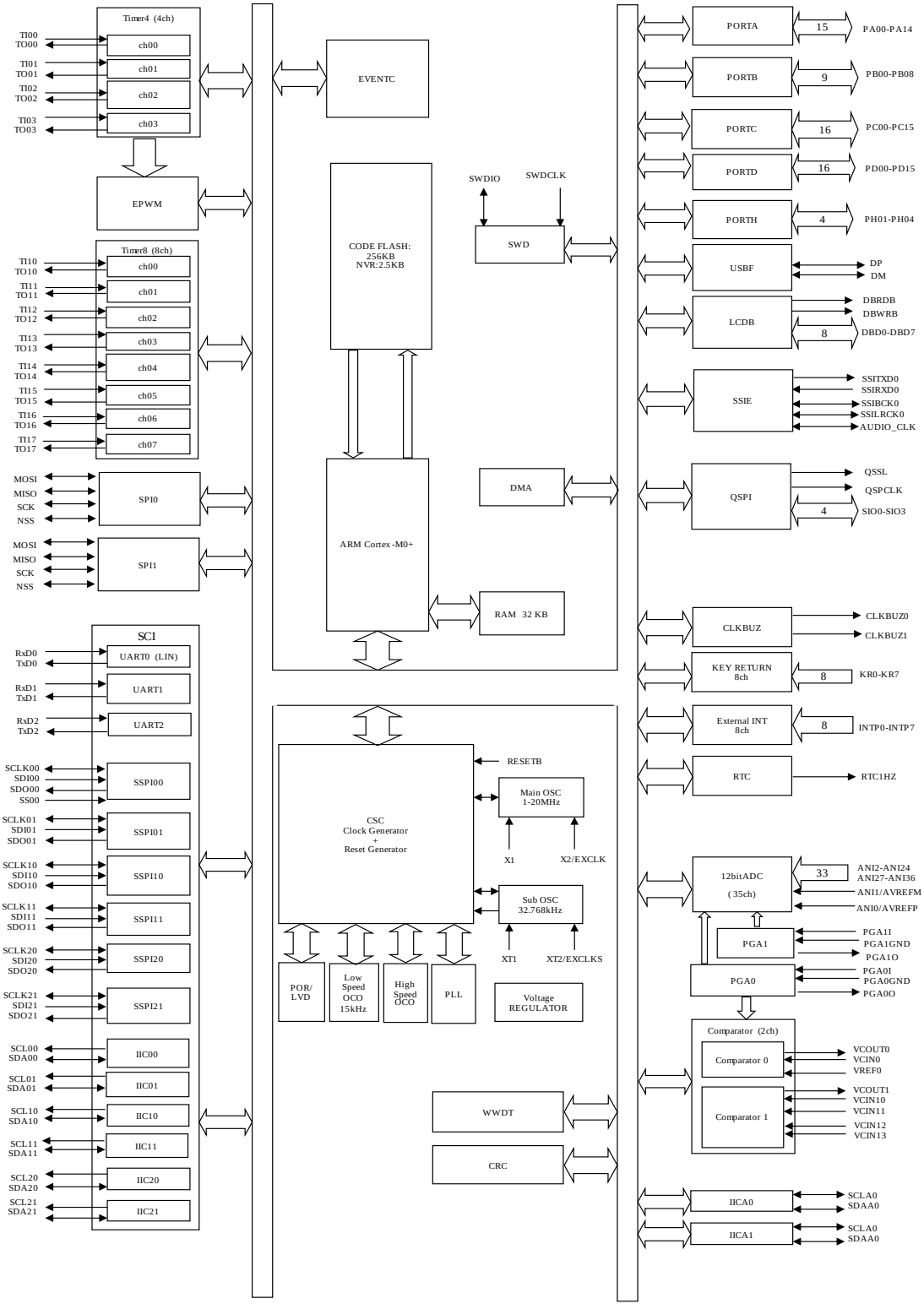
## 1.3.3 64 pin product – LQFP64

- 64-pin plastic package LQFP (7×7mm, 0.4mm pitch)




Note: The unmarked digital function support pins in the figure are configurable, see section 4.1 for details.

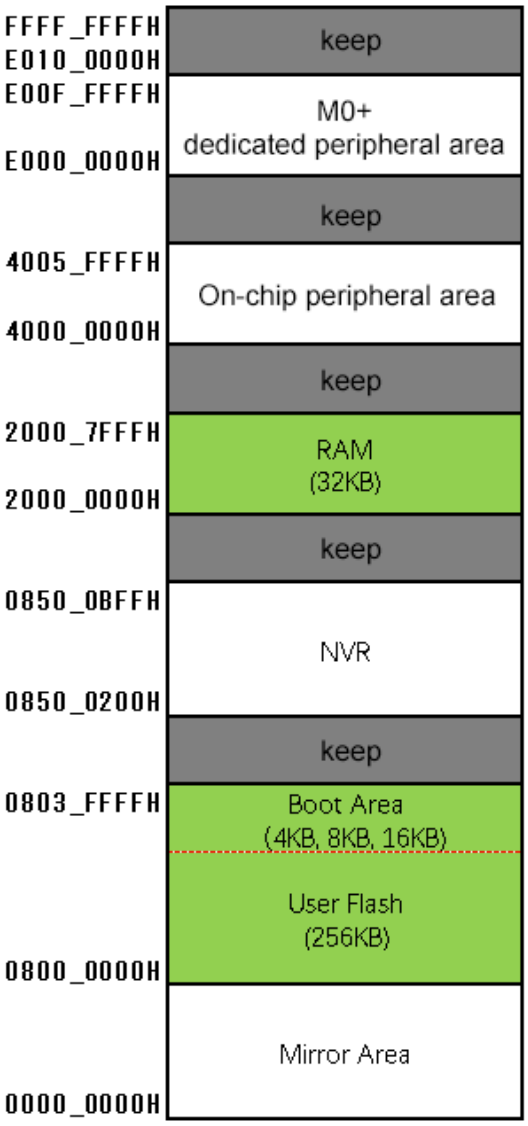
# 2 Product structure diagram




Note: The above is for 64 pin product. Some functions of products below 64 pin are not supported.

# 3 Memory mapping

#note:All green areas can be remapped to the mirrored area



# 4 Pin function

## 4.1 Port function

The functions of each port are shown in Table 4.1.1.

Table 4.1.1

| Port name | Reuse function | Digital output function set register pxxcfg[3:0] | Digital input function set register xxxPCFG[5:0] | Whether the function is equipped | |
|---|---|---|---|---|---|
| | | | | 64LQFP | 48LQFP 48QFN |
| RESETB | RESETB | - | - | ● | ● |
| PA00 | GPIO | 00H | 00H | ● | ● |
| | ANI0 | 00H | 00H | ● | ● |
| | VCIN10 | 00H | 00H | ● | ● |
| | CLKBUZ0 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PA01 | GPIO | 00H | 00H | ● | ● |
| | ANI1 | 00H | 00H | ● | ● |
| | VCIN11 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PA02 | GPIO | 00H | 00H | ● | ● |
| | ANI2 | 00H | 00H | ● | ● |
| | AVREFP | 00H | 00H | ● | ● |
| | VCIN12 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PA03 | GPIO | 00H | 00H | ● | ● |
| | ANI3 | 00H | 00H | ● | ● |
| | AVREFM | 00H | 00H | ● | ● |
| | VCIN13 | 00H | 00H | ● | ● |
| | SS00 | 00H | 00H | ● | ● |
| | PGA_ADJOUT | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PA04 | GPIO | 00H | 00H | ● | ● |
| | ANI4 | 00H | 00H | ● | ● |
| | VCIN0 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PA05 | GPIO | 00H | 00H | ● | ● |
| | ANI5 | 00H | 00H | ● | ● |
| | VREF0 | 00H | 00H | ● | ● |
| | PGA0IN | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PA06 | GPIO | 00H | 00H | ● | ● |

| | | | | | |
|---|---|---|---|---|---|
| | ANI6 | 00H | 00H | ● | ● |
| | PGA0GND | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PA07 | GPIO | 00H | 00H | ● | ● |
| | USB_DM | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PA08 | GPIO | 00H | 00H | ● | ● |
| | USB_DP | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PA09 | GPIO | 00H | 00H | ● | ● |
| | USB_VBUS | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PA10 | GPIO | 00H | 00H | ● | ● |
| | SCLK10 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PA11 | GPIO | 00H | 00H | ● | - |
| | ANI27 | 00H | 00H | ● | - |
| | SCLK00 | 00H | 00H | ● | - |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | - |
| PA12 | GPIO | 00H | 00H | ● | - |
| | ANI28 | 00H | 00H | ● | - |
| | SDO01 | 00H | 00H | ● | - |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | - |
| PA13 | GPIO | 00H | 00H | ● | - |
| | ANI29 | 00H | 00H | ● | - |
| | SDI01/SDA01 | 00H | 00H | ● | - |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | - |
| PA14 | GPIO | 00H | 00H | ● | - |
| | ANI30 | 00H | 00H | ● | - |
| | SCLK01/SCL01 | 00H | 00H | ● | - |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | - |
| PB00 | GPIO | 00H | 00H | ● | ● |
| | RTC1HZ | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PB01 | GPIO | 00H | 00H | ● | - |
| | ANI31 | 00H | 00H | ● | - |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | - |
| PB02 | GPIO | 00H | 00H | ● | - |
| | ANI32 | 00H | 00H | ● | - |
| | SCLK20 | 00H | 00H | ● | - |

| | | | | | |
|---|---|---|---|---|---|
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | - |
| PB03 | GPIO | 00H | 00H | ● | - |
| | ANI33 | 00H | 00H | ● | - |
| | SCLK21/SCL21 | 00H | 00H | ● | - |
| | SWCLK | 00H | 00H | ● | - |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | - |
| PB04 | GPIO | 00H | 00H | ● | - |
| | ANI34 | 00H | 00H | ● | - |
| | SDI21/SDA21 | 00H | 00H | ● | - |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | - |
| PB06 | GPIO | 00H | 00H | ● | ● |
| | ANI12 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PC00 | GPIO | 00H | 00H | ● | ● |
| | ANI15 | 00H | 00H | ● | ● |
| | SPI1_SCK | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PC01 | GPIO | 00H | 00H | ● | ● |
| | ANI16 | 00H | 00H | ● | ● |
| | SPI1_MOSI | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PC02 | GPIO | 00H | 00H | ● | ● |
| | ANI17 | 00H | 00H | ● | ● |
| | SPI1_MISO | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PC03 | GPIO | 00H | 00H | ● | ● |
| | ANI18 | 00H | 00H | ● | ● |
| | SPI0_SCK | 00H | 00H | ● | ● |
| | SCLK11/SCL11 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PC04 | GPIO | 00H | 00H | ● | ● |
| | ANI19 | 00H | 00H | ● | ● |
| | SPI0_MOSI | 00H | 00H | ● | ● |
| | SDO11 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PC05 | GPIO | 00H | 00H | ● | ● |
| | ANI20 | 00H | 00H | ● | ● |
| | SPI0_MISO | 00H | 00H | ● | ● |
| | SDI11/SDA11 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PC06 | GPIO | 00H | 00H | ● | ● |

| | | | | | |
|---|---|---|---|---|---|
| | ANI21 | 00H | 00H | ● | ● |
| | KR0 | 00H | 00H | ● | ● |
| | DBD0 | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | – |
| PC07 | GPIO | 00H | 00H | ● | ● |
| | ANI22 | 00H | 00H | ● | ● |
| | KR1 | 00H | 00H | ● | ● |
| | DBD1 | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PC08 | GPIO | 00H | 00H | ● | – |
| | ANI23 | 00H | 00H | ● | ● |
| | KR6 | 00H | 00H | ● | ● |
| | DBD6 | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PC09 | GPIO | 00H | 00H | ● | ● |
| | ANI24 | 00H | 00H | ● | – |
| | KR7 | 00H | 00H | ● | ● |
| | DBD7 | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PC10 | GPIO | 00H | 00H | ● | ● |
| | ANI25 | 00H | 00H | ● | ● |
| | DBRDB | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PC11 | GPIO | 00H | 00H | ● | ● |
| | ANI26 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| | KR4 | 00H | 00H | ● | – |
| | DBWRB | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | – |
| PC12 | GPIO | 00H | 00H | ● | – |
| | DBD2 | 00H | 00H | ● | – |
| | KR2 | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | – |
| PC13 | GPIO | 00H | 00H | ● | – |
| | DBD3 | 00H | 00H | ● | – |
| | KR3 | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | – |
| PC14 | GPIO | 00H | 00H | ● | – |
| | DBD4 | 00H | 00H | ● | – |
| | KR4 | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | – |

| | | | | | |
|---|---|---|---|---|---|
| PC15 | GPIO | 00H | 00H | ● | – |
| | DBD5 | 00H | 00H | ● | – |
| | KR5 | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | – |
| PD00 | GPIO | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PD01 | GPIO | 00H | 00H | ● | ● |
| | USB_VBUSEN | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PD02 | GPIO | 00H | 00H | ● | ● |
| | QSPCLK | 00H | 00H | ● | – |
| | SSIMCLK | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PD03 | GPIO | 00H | 00H | ● | ● |
| | QSSL | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PD04 | GPIO | 00H | 00H | ● | ● |
| | ANI7 | 00H | 00H | ● | ● |
| | USB_ID | 00H | 00H | ● | ● |
| | EPWMO00 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PD05 | GPIO | 00H | 00H | ● | ● |
| | ANI8 | 00H | 00H | ● | ● |
| | USB_EXICEN | 00H | 00H | ● | ● |
| | EPWMO01 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PD06 | GPIO | 00H | 00H | ● | ● |
| | ANI9 | 00H | 00H | ● | ● |
| | USB_OVRCURA | 00H | 00H | ● | ● |
| | EPWMO02 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PD07 | GPIO | 00H | 00H | ● | ● |
| | ANI10 | 00H | 00H | ● | ● |
| | USB_OVRCURB | 00H | 00H | ● | ● |
| | EPWMO03 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PD08 | GPIO | 00H | 00H | ● | ● |
| | ANI11 | 00H | 00H | ● | ● |
| | EPWMO04 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PD09 | GPIO | 00H | 00H | ● | ● |

| | | | | | |
|---|---|---|---|---|---|
| | EPWMO05 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PD10 | GPIO | 00H | 00H | ● | ● |
| | EPWMO06 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PD11 | GPIO | 00H | 00H | ● | ● |
| | EPWMO07 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PD12 | GPIO | 00H | 00H | ● | – |
| | QIO0 | 00H | 00H | ● | – |
| | SSIRXD0 | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | – |
| PD13 | GPIO | 00H | 00H | ● | – |
| | QIO1 | 00H | 00H | ● | – |
| | SSITXD0 | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | – |
| PD14 | GPIO | 00H | 00H | ● | – |
| | QIO2 | 00H | 00H | ● | – |
| | SSIRCK0/SSIFS | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | – |
| PD15 | GPIO | 00H | 00H | ● | – |
| | QIO3 | 00H | 00H | ● | – |
| | SSIBCK0 | 00H | 00H | ● | – |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | – |
| PH01 | GPIO | 00H | 00H | ● | ● |
| | X1 | 00H | 00H | ● | ● |
| | VCOUT0 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PH02 | GPIO | 00H | 00H | ● | ● |
| | X2 | 00H | 00H | ● | ● |
| | EXCLK | 00H | 00H | ● | ● |
| | VCOUT1 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PH03 | GPIO | 00H | 00H | ● | ● |
| | XT1 | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |
| PH04 | GPIO | 00H | 00H | ● | ● |
| | XT2 | 00H | 00H | ● | ● |
| | EXCLKS | 00H | 00H | ● | ● |
| | Configurable digital functions | X（see table 4.1.3） | X（see table 4.1.3） | ● | ● |

| | | | | | |
|---|---|---|---|---|---|
| VDD | Power supply | - | - | ● | ● |
| VSS | Ground | - | - | ● | ● |
| UVDD | Power supply | - | - | ● | ● |
| UVBUS | Power supply | - | - | ● | ● |

The digital function configuration of this product is to divide the 60 ports into three groups, GRP0, GRP1, and GRP2, and redirect part of the functions within the group. Port grouping see table 4.1.2, digital function configuration see table 4.1.3.

In addition to the default multiplexing function of the 20 ports in GRP0, the multiplexing functions of channel 0~channel 3 of the universal timer TIMER4, serial interface UART0 and serial interface IICA0 can also be redirected arbitrarily.

In addition to the default multiplexing function of the 20 ports in GRP1, the multiplexing functions of channel 0~channel 3 of the universal timer TIMER8, serial interface UART1 and high-speed SPI serial port SPIHS0 can also be redirected arbitrarily.

In addition to the default multiplexing function of the 20 ports in GRP2, the multiplexing functions of channel 4~channel 7 of the universal timer TIMER8, serial interface UART2, serial interface IICA1 and buzzer output CLKBUZ1 can also be redirected arbitrarily.

Table 4.1.2 Port grouping

| Serial number | GRP0 | GRP1 | GRP2 |
|---|---|---|---|
| 0 | PB00 | PC03 | PB01 |
| 1 | PH04 | PC04 | PB02 |
| 2 | PH03 | PC05 | PB03 |
| 3 | PH02 | PC06 | PB04 |
| 4 | PH01 | PC07 | PB05 |
| 5 | PC14 | PC12 | PB06 |
| 6 | PC15 | PC13 | PB07 |
| 7 | PC08 | PA04 | PB08 |
| 8 | PC09 | PA05 | PC00 |
| 9 | PC10 | PA06 | PC01 |
| 10 | PC11 | PA07 | PC02 |
| 11 | PA00 | PA08 | PA11 |
| 12 | PA01 | PA09 | PA12 |
| 13 | PA02 | PA10 | PA13 |
| 14 | PA03 | PD00 | PA14 |
| 15 | PD07 | PD01 | PD02 |
| 16 | PD08 | PD12 | PD03 |
| 17 | PD09 | PD13 | PD04 |
| 18 | PD10 | PD14 | PD05 |
| 19 | PD11 | PD15 | PD06 |

Table 4.1.3 List of digital function configuration (1/2 output function configuration)

| Pin | Control register | Register configuration | Pin dual-purpose function |
|---|---|---|---|
| GRP0 | PB00CFG/PH04CFG/PH03CFG/PH02CFG/ PH01CFG/PC14CFG/PC15CFG/PC08CFG/ PC09CFG/PC10CFG/PC11CFG/PA00CFG/ PA01CFG/PA02CFG/PC03CFG/PD07CFG/ PD08CFG/PD09CFG/PF10CFG/PD11CFG | 4'h00 | GPIO/default dual-purpose output |
| | | 4'h01 | TO00 |
| | | 4'h02 | TO01 |
| | | 4'h03 | TO02 |
| | | 4'h04 | TO03 |
| | | 4'h05 | SDO00/TxD0 |
| | | Others | Prohibited to set |
| GRP1 | PC03CFG/PC04CFG/PC05CFG/PC06CFG/ PC07CFG/PC12CFG/PC13CFG/PA04CFG/ PA05CFG/PA06CFG/PA07CFG/PA08CFG/ PA09CFG/PA10CFG/PD00CFG/PD01CFG/ PD12CFG/PD13CFG/PD14CFG/PD15CFG | 4'h00 | GPIO/default dual-purpose output |
| | | 4'h01 | TO10 |
| | | 4'h02 | TO11 |
| | | 4'h03 | TO12 |
| | | 4'h04 | TO13 |
| | | 4'h05 | TxD1/IrTxD/SDO10 |
| | | 4'h06 | SPIHS0_SCKO |
| | | 4'h07 | SPIHS0_MO |
| | | 4'h08 | SPIHS0_SO |
| | | Others | Prohibited to set |
| GRP2 | PB01CFG/PB02CFG/PB03CFG/PB04CFG/ PB05CFG/PB06CFG/PB07CFG/PB08CFG/ PC00CFG/PC01CFG/PC02CFG/PA11CFG/ PA12CFG/PA13CFG/PA14CFG/PD02CFG/ PD03CFG/PD04CFG/PD05CFG/PD06CFG | 4'h00 | GPIO/default dual-purpose output |
| | | 4'h01 | TO14 |
| | | 4'h02 | TO15 |
| | | 4'h03 | TO16 |
| | | 4'h04 | TO17 |
| | | 4'h05 | TxD2/SDO20 |
| | | 4'h06 | CLKBUZ1 |
| | | Others | Prohibited to set |

Table 4.1.3 Digital function configuration list (2/2 input function configuration)

| Grouping | Control register | Register configuration | Pin dual-purpose function |
|---|---|---|---|
| GRP0 | TI00PCFG<br>TI01PCFG<br>TI02PCFG<br>TI33PCFG<br>RXD0PCFG(UART)<br>SCLA0PCFG(IICA0)<br>SDAA0PCFG(IICA1) | 6'h00 | Default dual-purpose input |
| | | 6'h01 | PB00 as a dual input |
| | | 6'h02 | PH04 as a dual input |
| | | 6'h03 | PH03 as a dual input |
| | | 6'h04 | PH02 as a dual input |
| | | 6'h05 | PH01 as a dual input |
| | | 6'h06 | PC14 as a dual input |
| | | 6'h07 | PC15 as a dual input |
| | | 6'h08 | PC08 as a dual input |
| | | 6'h09 | PC09 as a dual input |
| | | 6'h0a | PC10 as a dual input |
| | | 6'h0b | PC11 as a dual input |
| | | 6'h0c | PA00 as a dual input |
| | | 6'h0d | PA01 as a dual input |
| | | 6'h0e | PA02 as a dual input |
| | | 6'h0f | PA03 as a dual input |
| | | 6'h10 | PD07 as a dual input |
| | | 6'h11 | PD08 as a dual input |
| | | 6'h12 | PD09 as a dual input |
| | | 6'h13 | PD10 as a dual input |
| | | 6'h14 | PD11 as a dual input |
| | | Others | Prohibited to set |
| GRP1 | TI10PCFG<br>TI11PCFG<br>TI12PCFG<br>TI13PCFG<br>RXD1PCFG(UART)<br>SPIHS0_SCKIPCFG(SPI)<br>SPIHS0_SIPCFG(SPI)<br>SPIHS0_MIPCFG(SPI) | 6'h00 | Default dual-purpose input |
| | | 6'h01 | PC03 as a dual input |
| | | 6'h02 | PC04 as a dual input |
| | | 6'h03 | PC05 as a dual input |
| | | 6'h04 | PC06 as a dual input |
| | | 6'h05 | PC07 as a dual input |
| | | 6'h06 | PC12 as a dual input |
| | | 6'h07 | PC13 as a dual input |
| | | 6'h08 | PA04 as a dual input |
| | | 6'h09 | PA05 as a dual input |
| | | 6'h0a | PA06 as a dual input |
| | | 6'h0b | PA07 as a dual input |
| | | 6'h0c | PA08 as a dual input |
| | | 6'h0d | PA09 as a dual input |
| | | 6'h0e | PA10 as a dual input |

| | | | |
|---|---|---|---|
| | | 6’h0f | PD00 as a dual input |
| | | 6’h10 | PD01 as a dual input |
| | | 6’h11 | PD12 as a dual input |
| | | 6’h12 | PD13 as a dual input |
| | | 6’h13 | PD14 as a dual input |
| | | 6’h14 | PD15 as a dual input |
| | | Others | Prohibited to set |
| GRP2 | TI14PCFG<br>TI15PCFG<br>TI16PCFG<br>TI17PCFG<br>RXD2PCFG(UART)<br>SPIHS1_NSSPCFG(SPI)<br>SCLA1PCFG(IICA1)<br>SDA1PCFG(IICA1) | 6’h00 | Default dual-purpose input |
| | | 6’h01 | PB01 as a dual input |
| | | 6’h02 | PB02 as a dual input |
| | | 6’h03 | PB03 as a dual input |
| | | 6’h04 | PB04 as a dual input |
| | | 6’h05 | PB05 as a dual input |
| | | 6’h06 | PB06 as a dual input |
| | | 6’h07 | PB07 as a dual input |
| | | 6’h08 | PB08 as a dual input |
| | | 6’h09 | PC00 as a dual input |
| | | 6’h0a | PC01 as a dual input |
| | | 6’h0b | PC02 as a dual input |
| | | 6’h0c | PA11 as a dual input |
| | | 6’h0d | PA12 as a dual input |
| | | 6’h0e | PA13 as a dual input |
| | | 6’h0f | PA14 as a dual input |
| | | 6’h10 | PD02 as a dual input |
| | | 6’h11 | PD03 as a dual input |
| | | 6’h12 | PD04 as a dual input |
| | | 6’h13 | PD05 as a dual input |
| | | 6’h14 | PD06 as a dual input |
| | | Others | Prohibited to set |

Table 4.1.3 List of External Interrupt Pin Function Configuration

| Pin | Control register | Register configuration | External interrupt port selection |
|---|---|---|---|
| INTP0 | INTP0PCFG | 3'h00 | PC00 |
| | | 3'h01 | PC01 |
| | | 3'h02 | PC02 |
| | | 3'h03 | PC03 |
| | | 3'h04 | PC04 |
| | | 3'h05 | PC05 |
| | | 3'h06 | PC06 |
| | | 3'h07 | PC07 |
| INTP1 | INTP1PCFG | 3'h00 | PC12 |
| | | 3'h01 | PC13 |
| | | 3'h02 | PC14 |
| | | 3'h03 | PC15 |
| | | 3'h04 | PC08 |
| | | 3'h05 | PC09 |
| | | 3'h06 | PC10 |
| | | 3'h07 | PC11 |
| INTP2 | INTP2PCFG | 3'h00 | PA00 |
| | | 3'h01 | PA01 |
| | | 3'h02 | PA02 |
| | | 3'h03 | PA03 |
| | | 3'h04 | PA11 |
| | | 3'h05 | PA12 |
| | | 3'h06 | PA13 |
| | | 3'h07 | PA14 |
| INTP3 | INTP3PCFG | 3'h00 | PA04 |
| | | 3'h01 | PA05 |
| | | 3'h02 | PA06 |
| | | 3'h03 | PA07 |
| | | 3'h04 | PA08 |
| | | 3'h05 | PA09 |
| | | 3'h06 | PA10 |
| | | Others | Prohibited to set |
| INTP4 | INTP4PCFG | 3'h00 | PD00 |
| | | 3'h01 | PD01 |
| | | 3'h02 | PD12 |
| | | 3'h03 | PD13 |
| | | 3'h04 | PD14 |
| | | 3'h05 | PD15 |
| | | 3'h06 | PD02 |
| | | 3'h07 | PD03 |
| INTP5 | INTP5PCFG | 3'h00 | PD04 |

| | | | |
|---|---|---|---|
| | | 3’h01 | PD05 |
| | | 3’h02 | PD06 |
| | | 3’h03 | PD07 |
| | | 3’h04 | PD08 |
| | | 3’h05 | PD09 |
| | | 3’h06 | PD10 |
| | | 3’h07 | PD11 |
| INTP6 | INTP6PCFG | 3’h00 | PB00 |
| | | 3’h01 | PH04 |
| | | 3’h02 | PH03 |
| | | 3’h03 | PH02 |
| | | 3’h04 | PH01 |
| | | 3’h05 | PB01 |
| | | 3’h06 | PB02 |
| | | Others | Prohibited to set |
| INTP7 | INTP7PCFG | 3’h00 | PB03 |
| | | 3’h01 | PB04 |
| | | 3’h02 | PB05 |
| | | 3’h03 | PB06 |
| | | 3’h04 | PB07 |
| | | 3’h05 | PB08 |
| | | Others | Prohibited to set |

## 4.2 Port multiplexing function

（1/2）

| Function name | input/output | Function |
|---|---|---|
| ANI0～ANI34 | input | Analog input of A/D converter |
| INTP0～INTP7 | input | External interrupt request input. Designation of valid edges: rising edge, falling edge, rising and falling double edges |
| VCIN0 | input | Analog voltage input of comparator 0 |
| VCIN10, VCIN11, VCIN12, VCIN13 | input | Comparator1's analog voltage/reference voltage input |
| VREF0 | input | Reference voltage input of comparator0 |
| VCOUT0、VCOUT1 | output | Comparator output |
| PGA0IN | input | PGA input |
| PGA0_ADJOUT | output | PGA output |
| PGA0GND | input | PGA reference input |
| KR0～KR7 | input | Key interrupt input |
| CLKBUZ0、CLKBUZ1 | output | Clock output / buzzer output |
| RTC1HZ | output | Real-time clock correction clock (1Hz) output |
| RESETB | input | Low-level active system reset input. When external reset is not used, it must be connected to VDD directly or through a resistor. |
| RxD0～RxD2 | input | Serial data input of serial interface UART0, UART1, UART2 |
| TxD0～TxD2 | output | Serial data output of serial interface UART0, UART1, UART2 |
| SCL00、SCL01、SCL10、SCL11、SCL20、SCL21 | output | Serial clock output of serial interface IIC00, IIC01, IIC10, IIC11, IIC20, IIC21 |
| SDA00、SDA01、SDA10、SDA11、SDA20、SDA21 | input/output | Serial data input/output of serial interface IIC00, IIC01, IIC10, IIC11, IIC20, IIC21 |
| SCLK00、SCLK01、SCLK10、SCLK11、SCLK20、SCLK21 | input/output | Serial clock input/output of serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21 |
| SDI00、SDI01、SDI10、SDI11、SDI20、SDI21 | input | Serial data input of serial interface SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21 |
| SS00 | input | Chip selection input of serial interface SSPI00 |
| SDO00、SDO01、SDO10、SDO11、SDO20、SDO21 | output | Serial data output of SSPI00, SSPI01, SSPI10, SSPI11, SSPI20, SSPI21 |
| DBD0~DBD7 | input/ output | LCD bus data input/output |
| DBRDB | output | LCD bus read enable output |
| DBWRB | output | LCD bus write enable output |
| QIO0~QIO3 | input/ output | QSPI data input/output |
| QSPCLK | output | QSPI clock output |
| QSSL | output | QSPI slave select |
| SPIHS0_NSS | input | Chip select input of serial interface SPIHS0 |
| SPIHS0_SCK | input/output | Serial clock input/output of serial interface SPIHS0 |
| SPIHS0_MISO | input/output | Serial data input/output of serial interface SPIHS0 |

（2/2）

| Function name | input/ output | Function |
|---|---|---|
| SPIHS0_MOSI | input/output | Serial data input/output of serial interface SPIHS0 |
| SPIHS1_NSS | input | Chip select input of serial interface SPIHS1 |
| SPIHS1_SCK | input/output | Serial clock input/output of serial interface SPIHS1 |
| SPIHS1_MISO | input/output | Serial data input/output of serial interface SPIHS1 |
| SPIHS1_MOSI | input/output | Serial data input/output of serial interface SPIHS1 |
| SCLA0 | input/output | Clock input/output of serial interface IICA0 |
| SDAA0 | input/output | Serial data input/output of serial interface IICA0 |
| SCLA1 | input/output | Clock input/output of serial interface IICA1 |
| SDAA1 | input/output | Serial data input/output of serial interface IICA1 |
| TI00～TI03 | input | 16-bit timer Timer4 external count clock/capture trigger input |
| TO00～TO03 | output | Timer output of 16-bit timer Timer4 |
| TI10～TI17 | input | 16-bit timer Timer8 external count clock/capture trigger input |
| TO10～TO17 | output | Timer output of 16-bit timer Timer8 |
| USB_VBUSEN | output | VBUS enable signal from USB output to external power IC |
| USB_ID | input | ID input signal connected to MicroAB connector in OTG mode |
| USB_EXICEN | output | Output low power control signal to OTG power IC |
| USB_OVRCUA、USB_OVRCUB | input | Overcurrent port |
| USB_DP | input/output | D+ line De of USB transceiver |
| USB_DM | input/output | D-line of USB transceiver |
| USB_VBUS | input | USB connection detection port |
| UVDD | input/output | input: the power supply of the USB transceiver, output: the output port of the USB LDO. |
| SSIRXD0 | input | Send data of serial audio interface SSI |
| SSITXD0 | output | Receive data of serial audio interface SSI |
| SSILRCK0/SSIFS | input/output | Frame clock/frame synchronization of serial audio interface SSI |
| SSIBCK0 | input/output | Serial audio interface SSI bit clock |
| SSIMCLK | input | The main clock of the serial audio interface SSI |
| X1、X2 | — | Connect the resonator for the main system clock. |
| EXCLK | input | External clock input of main system clock |
| XT1、XT2 | — | Connect the resonator for the subsystem clock. |
| EXCLKS | input | External clock input for subsystem clock |
| VDD | — | Power supply |
| AVREFP | input | Positive (+) reference voltage input of A/D converter |
| AVREFM | input | Negative (–) reference voltage input of A/D converter |
| VSS | — | Groud |
| SWDIO | input/output | SWD data interface |
| SWCLK | input | SWD clock interface |

Remark: As a countermeasure for noise and locking, the bypass capacitor (about 0.1uF) must be connected with the shortest distance between VDD and VSS and thicker wiring.

# 5 Function summary

## 5.1 ARM® Cortex®-M0+ core

ARM's Cortex-M0(+) processor is a new generation of ARM processors for embedded systems. It provides a low-cost platform designed to meet the needs of a small pin count and low-power microcontroller, while providing excellent computing performance and advanced system response to interrupts.

The 32-bit RISC processor of the Cortex-M0(+) processor provides excellent code efficiency and the expected high performance of the ARM core, which is different from 8-bit and 16-bit devices of the same memory size. The Cortex-M0(+) processor has 32 address lines and a storage space of up to 4G.

BAT32G157 uses an embedded ARM core, so it is compatible with all ARM tools and software.

## 5.2 Memory

### 5.2.1 Flash

BAT32G157 has a built-in flash memory that can be programmed, erased and rewritten. Has the following functions:

- Programs and data share 256K storage space.
- 2.5KB dedicated data Flash memory
- Support page erasing, each page size is 512byte, erasing time 4ms
- Support byte/half-word/word (32bit) programming, programming time 24us

### 5.2.2 SRAM

BAT32G157 has built-in 32K bytes of embedded SRAM.

## 5.3 Enhanced DMA controller

Built-in enhanced DMA (Direct Memory Access) controller can realize the function of data transfer between memories without using CPU.

- It supports the start of DMA through peripheral function interrupts, and can realize real-time control through communication, timer and A/D.
- The transmission source/destination area is optional for the entire address space range (when the flash area is used as the destination address, the flash needs to be preset to the programming mode).
- Supports 4 transfer modes (normal transfer mode, repetitive transfer mode, block transfer mode and chain transfer mode).

## 5.4 Linkage controller

The linkage controller links each peripheral function output event with the peripheral function trigger source. So as to realize the coordinated operation between peripheral functions without using the CPU.

The linkage controller has the following functions:

- The event signals can be linked together to realize the linkage of peripheral functions.
- 15 types of event input, 4 types of event trigger.

## 5.5 Clock generation and start

The clock generation circuit is a circuit that generates a clock for the CPU and peripheral hardware. There are the following 4 types of system clocks and clock oscillation circuits.

### 5.5.1 Main system clock

- X1 oscillator circuit: It can generate 1-20MHz clock oscillation by connecting a resonator to the pins (X1 and X2), and can stop the oscillation by executing a deep sleep command or setting MSTOP.
- High-speed internal oscillator (high-speed OCO): The frequency can be selected for oscillation by the option byte. After the reset is released, the CPU defaults to start running with this high-speed internal oscillator clock. Oscillation can be stopped by executing a deep sleep instruction or setting the HIOSTOP bit. The frequency set by the option byte can be changed through the frequency selection register of the high-speed internal oscillator. The highest frequency is 64Mhz, and the accuracy is ±1.0%.
- Input the external clock from the pin (X2): (1～20MHz), and the input of the external main system clock can be disabled by executing the deep sleep instruction or setting the MSTOP bit.

### 5.5.2 Subsystem clock

- XT1 oscillator circuit: It can generate 32.768kHz clock oscillation by connecting a 32.768kHz resonator to the pins (XT1 and XT2), and the oscillation can be stopped by setting the XTSTOP bit.
- Input the external clock from the pin (XT2): 32.768kHz, and the input of the external clock can be disabled by setting the XTSTOP bit.

### 5.5.3 Low-speed internal oscillator clock

- Low-speed internal oscillator (low-speed OCO): generates 15kHz (TYP.) clock oscillation. The low-speed internal oscillator clock can be used as the CPU clock. The following peripheral hardware can be run by the low-speed internal oscillator clock:
- Watchdog timer（WWDT）
- Real Time Clock（RTC）
- 15-bit interval timer

### 5.5.4 PLL

- Built-in two PLLs: one is for system clock and the other is for USB. The source clock of the PLL can be either an external clock or a high-speed internal oscillator clock.

## 5.6 Power management

### 5.6.1 Power supply mode

VDD: external power supply, voltage range 1.8 to 5.5V

### 5.6.2 Power-on reset

The power-on reset circuit (POR) has the following functions:

- An internal reset signal is generated when the power is turned on. If the power supply voltage (VDD) is greater than the detection voltage (VPOR), the reset is released. However, before reaching the operating voltage range, the reset state must be maintained through a voltage detection circuit or an external reset.
- The power supply voltage (VDD) and the detection voltage (VPDR) are compared. When VDD<VPDR, an internal reset signal is generated. However, when the power supply drops, it must be shifted to the deep sleep mode before it falls below the operating voltage range, or set to the reset state through a voltage detection circuit or an external reset. If you want to restart operation, you must confirm that the power supply voltage has returned to the operating voltage range.

### 5.6.3 Voltage detection

The voltage detection circuit sets the operation mode and detection voltage (VLVDH, VLVDL, VLVD) through the option byte. The voltage detection (LVD) circuit has the following functions:

- Compare the power supply voltage (VDD) with the detection voltage (VLVDH, VLVDL, VLVD) and generate an internal reset or interrupt request signal.
- The detection voltage of the power supply voltage (VLVDH, VLVDL, VLVD) can select the detection level by the option byte.
- Can run in deep sleep mode.
- When the power supply rises, before reaching the operating voltage range, the reset state must be maintained through a voltage detection circuit or an external reset. When the power supply drops, it must be transferred to the deep sleep mode before being lower than the operating voltage range, or set to the reset state through a voltage detection circuit or an external reset.
- The operating voltage range varies according to the setting of the user option byte.

## 5.7 Low power consumption mode

BAT32G157 supports two low-power modes to achieve the best compromise between low power consumption, short startup time, and available wake-up sources:

- Sleep mode: Enter the sleep mode by executing the sleep command. The sleep mode is a mode in which the CPU operating clock is stopped. Before setting the sleep mode, if the high-speed system clock oscillator circuit, high-speed internal oscillator, or subsystem clock oscillator circuit is oscillating, each clock continues to oscillate. Although this mode cannot reduce the operating current to the level of the

deep sleep mode, it is an effective mode when you want to restart processing immediately through an interrupt request or when you want to perform intermittent operation frequently.

- Deep sleep mode: Enter the deep sleep mode by executing the deep sleep command. The deep sleep mode is a mode to stop the oscillation of the high-speed system clock oscillation circuit and the high-speed internal oscillator and stop the entire system. Can greatly reduce the operating current of the chip. Because the deep sleep mode can be cancelled by an interrupt request, intermittent operation is also possible. However, in the case of the X1 clock, because it is necessary to ensure the wait time for stable oscillation when releasing the deep sleep mode, if you must start processing immediately with an interrupt request, you must select the sleep mode.

In either mode, the registers, flags, and data memory all retain the contents before the standby mode, and also maintain the status of the output latch and output buffer of the input/output port.

## 5.8 Reset function

The following 7 methods to generate a reset signal:

1) Input external reset through RESETB pin.
2) Generate an internal reset through the program runaway detection of the watchdog timer.
3) The internal reset is generated by comparing the power supply voltage of the power-on reset (POR) circuit and the detection voltage.
4) The internal reset is generated by comparing the power supply voltage of the voltage detection circuit (LVD) and the detection voltage.
5) Internal reset due to RAM parity error.
6) Internal reset due to access to illegal memory.
7) Software reset

The internal reset is the same as the external reset. After the reset signal is generated, the program is executed from the addresses written in addresses 0000H and 0001H.

## 5.9 Interrupt function

The Cortex-M0+ processor has a built-in nested vectored interrupt controller (NVIC), which supports up to 32 interrupt request (IRQ) inputs and 1 non-maskable interrupt (NMI) input. In addition, the processor also supports multiple internal exceptions.

This product has processed 32 maskable interrupt requests (IRQ) and 1 non-maskable interrupt (NMI). For details, please refer to the corresponding chapters of the user manual. The actual number of interrupt sources varies by product.

## 5.10 Real time clock（RTC）

The real-time clock (RTC) has the following functions.

- Counter with year, month, week, day, hour, minute and second.
- Fixed period interrupt function (period: 0.5 second, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm clock: week, hour, minute)
- 1Hz pin output function
- Support the division of the subsystem clock or the main system clock as the running clock of the RTC
- The real-time clock interrupt signal (INTRTC) can be used as a wake-up from deep sleep mode
- Support a wide range of clock correction functions

Only when the sub-system clock (32.768kHz) or the divided frequency of the main system clock is selected as the running clock of the RTC, the year, month, week, day, hour, minute and second can be counted. When the low-speed internal oscillator clock (15kHz) is selected, only the fixed cycle interrupt function can be used.

## 5.11 Watchdog timer

1 channel WWDT, 17bit watchdog timer is set to count operation by option byte. The watchdog timer runs on the low-speed internal oscillator clock (15kHz). The watchdog timer is used to detect program runaway. When a program out of control is detected, an internal reset signal is generated.

The following conditions are judged to be out of control of the program:

- When the watchdog timer counter overflows
- When a 1-bit operation instruction is executed on the enable register (WDTE) of the watchdog timer
- When writing data other than "ACH" to the WDTE register
- When writing data to the WDTE register while the window is closed

## 5.12 SysTick timer

This timer is dedicated to the real-time operating system, but it can also be used as a standard down counter.

Its characteristics are: when the 24-bit down counter self-filling capacity counter reaches 0, a maskable system interrupt is generated.

## 5.13 Timer timer4/timer8

This product has a built-in timer unit timer4 with 4-channel 16-bit timer and a timer unit timer8 with 8-channel 16-bit customized timer. Each 16-bit timer is called a "channel", which can be used as an independent timer or combined with multiple channels for advanced timer functions.

For details of each function, please refer to the table below:

| Independent channel operation function | Multi-channel linkage operation function |
|---|---|
| ● Interval timer<br>● Square wave output<br>● External event counter<br>● Frequency divider<br>● Measurement of input pulse interval<br>● Measurement of the high/low level width of the input signal<br>● Delay counter | ● One-shot pulse output<br>● PWM output<br>● Multiple PWM output |

### 5.13.1 Independent channel operation function

The independent channel operation function is a function that can independently use any channel without being affected by the operation mode of other channels. The independent channel operation function can be used in the following modes:

1) Interval timer：Can be used as a reference timer that generates interrupts (INTTM) at regular intervals.
2) Square wave output：Whenever an INTTM interrupt is generated, a flip is triggered, and a square wave with a 50% duty cycle is output from the timer output pin (TO).
3) External event counter：Count the valid edge of the input signal of the timer input pin (TI), and if it reaches the specified number of times, it can be used as an event counter to generate an interrupt.
4) Frequency divider function (only limited to channel 0 of unit 0): divide the input clock of the timer input pin (TI00), and then output from the output pin (TO00).
5) Input pulse interval measurement: start counting at the valid edge of the input pulse signal of the timer input pin (TI) and capture the count value at the valid edge of the next pulse to measure the interval of the input pulse.
6) Measurement of the high/low level width of the input signal: start counting on one edge of the input signal of the timer input pin (TI) and capture the count value on the other edge to measure the high or low level of the input signal Width.
7) Delay counter: start counting at the valid edge of the input signal of the timer input pin (TI) and generate an interrupt after any delay period has elapsed.

### 5.13.2 Multi-channel linkage operation function

Multi-channel linkage operation function can be realized by combining the master channel (the basic timer of the main control cycle) and the slave channel (the timer that follows the master control channel). Multi-channel linkage operation function can be used in the following modes:

1) One-shot pulse output: Use two channels in pairs to generate one-shot pulses that can set the output timing and pulse width arbitrarily.
2) PWM (Pulse Width Modulation) output: Use 2 channels in pairs to generate pulses with a period and duty cycle that can be set arbitrarily.
3) Multiple PWM (Pulse Width Modulation) output: It can generate up to 7 kinds of PWM signals with any duty cycle in a fixed cycle by expanding the PWM function and using 1 master channel and multiple slave channels.

### 5.13.3 8-bit timer operation function

The 8-bit timer operation function can use the 16-bit timer channel as a function of two 8-bit timer channels. (Only channel 1 and channel 3 can be used)

### 5.13.4 LIN-bus support function

The timer4 unit can be used to check whether the received signal in LIN-bus communication is suitable for the LIN-bus communication format.

1) Wake-up signal detection: Start counting on the falling edge of the input signal of the UART serial data input pin (RxD) and capture the count value on the rising edge to measure the low-level width. If the low-level width is greater than or equal to a certain fixed value, it is considered as a wake-up signal.
2) Interval field detection: After detecting the wake-up signal, start counting from the falling edge of the input signal of the UART serial data input pin (RxD) and capture the count value on the rising edge to measure the low-level width. If the width of the low level is greater than or equal to a certain fixed value, it is regarded as an interval field.
3) Synchronous field pulse width measurement: After detecting the interval field, measure the low-level width and high-level width of the input signal of the UART serial data input pin (RxD). Calculate the baud rate based on the bit interval of the sync field measured in this way.

## 5.14 EPWM output control circuit

Use Timer4's PWM output function to control one DC motor or two stepping motors. By truncating the source CMP0 output, INTP0 input and EVENTC events, the output can be truncated. Through the setting of the software, you can choose from four types of output that are Hi-Z output, low-level output, high-level output, and forbidden cut-off output.。

## 5.15 15-bit interval timer

This product has a built-in 15-bit interval timer, which can generate interrupts (INTIT) at any time interval set in advance, and can be used to wake up from deep sleep mode.

## 5.16 Clock output/buzzer output control circuit

The clock output controller is used to provide the clock to the peripheral IC, and the buzzer output controller is used to output the square wave of the buzzer frequency. Clock output or buzzer output is realized by dedicated pins.

## 5.17 Universal serial communication unit（SCI）

This product has two built-in universal serial communication units, and each unit has up to 4 serial communication channels. It can realize the communication functions of standard SPI, simple SPI, UART and simple I2C. Take the 64pin product as an example, the function allocation of each channel is as follows:

### 5.17.1 3-wire serial interface（simple SPI）

Synchronize data transmission and reception with the serial clock (SCK) output from the master control device.

This is a clock synchronous communication interface that uses 1 serial clock (SCK), 1 sending serial data (SO), and 1 receiving serial data (SI) to communicate with a total of 3 communication lines.

[data transmission and reception]

- 7-bit or 8-bit data length
- Phase control of sending and receiving data
- MSB/LSB priority choice

[clock control]

- Choice of master control or slave
- Phase control of input/output clock
- The transmission cycle generated by the prescaler and the internal counter of the channel
- Maximum transfer rate

Master communication: Max.fCLK/2

Slave communication: Max.fMCK/6

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt

[Error detection flag]

- Overflow error

### 5.17.2 Simple SPI with slave chip select function

SPI serial communication interface supporting slave chip select input function. This is a clock synchronization that uses a slave chip select input (SSI), a serial clock (SCK), a sending serial data (SO), and a receiving serial data (SI) 4 communication lines for communication. Communication Interface.

[Data sending and receiving]

- 7-bit or 8-bit data length
- Phase control of sending and receiving data
- MSB/LSB priority choice
- Level setting of sending and receiving data

[clock control]

- Phase control of input/output clock
- The transmission cycle generated by the prescaler and the internal counter of the channel
- Maximum transfer rate

Slave communication: Max.fMCK/6

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt

[Error detection flag]

- Overflow error

### 5.17.3 UART

The function of asynchronous communication through two lines of serial data transmission (TxD) and serial data reception (RxD). Use these two communication lines to send and receive data asynchronously (using the internal baud rate) with other communication parties according to the data frame (consisting of start bit, data, parity bit and stop bit). Full-duplex UART communication can be realized by using two channels dedicated for transmission (even-numbered channels) and dedicated for reception (odd-numbered channels), and LIN-bus can be supported by combining timer4 units and external interrupts (INTP0).

[Data sending and receiving]

- 7-bit, 8-bit or 9-bit data length
- MSB/LSB priority choice
- Selection of level setting and reverse phase of sending and receiving data
- Additional parity check bit, parity check function
- Additional stop bit, stop bit detection

[Interrupt function]

- Transmission end interrupt, buffer empty interrupt
- Error interrupt caused by framing error, parity error or overflow error

[Error detection flag]

- Frame error, parity error, overflow error

[LIN-bus function]

- Wake-up signal detection
- BF detection
- Measurement of synchronization field, calculation of baud rate

### 5.17.4 Simple I2C

The function of clock synchronization communication with multiple devices through two lines of serial clock (SCL) and serial data (SDA). Because this simple I2C is designed for single communication with flash memory, A/D converters and other devices, it can only be used as a master device. The start condition and stop condition are the same as the operation control register, and must comply with the AC characteristics and be processed by software.

[ Data sending and receiving]

- Main control sending, main control receiving (only limited to the main control function of single main control)
- ACK output function, ACK detection function
- 8-bit data length (when sending the address, use the upper 7 bits to specify the address, and use the lowest bit for R/W control)
- Generate start and stop conditions through software

[ interrupt function]

- End of transmission interrupt

[ Error detection flag]

- ACK error, overflow error

[ Functions not supported by simple I2C]]

- Slave sending, slave receiving
- Multi-master control function (arbitration failure detection function)
- Waiting for detection function

## 5.18 Standard serial peripheral interface（SPI）

The serial interface SPI has the following 2 modes:

- Operation stop mode: This is a mode used when serial transmission is not performed, which can reduce power consumption
- 3-wire serial I/O mode: This mode uses 3 lines of serial clock (SCK) and serial data bus (MISO and MOSI) to transmit 8-bit or 16-bit data with multiple devices.

## 5.19 Standard serial interface（IICA）

The serial interface IICA has the following 3 modes:

- Operation stop mode: This is a mode used when serial transmission is not performed, which can reduce power consumption.
- I2C bus mode (supports multiple masters): This mode uses 2 lines of serial clock (SCLA) and serial data bus (SDAA) to transmit 8-bit data with multiple devices. In line with the I2C bus format, the master device can generate "start condition", "address", "indication of the transfer direction", "data" and "stop condition" for the slave device on the serial data bus. The slave device automatically detects the received status and data through hardware. This function can simplify the I2C bus control part of the application. Because the SCLA pin and SDAA pin of the serial interface IICA are used as open-drain output, the serial clock line and the serial data bus require a pull-up resistor.
- Wake-up mode: In the deep sleep mode, when the extension code or the local station address from the autonomous control device is received, the deep sleep mode can be released by generating an interrupt request signal (INTIICA). Set through the IICA control register.

## 5.20 LCD BUS interface

The LCD bus interface has the following functions:

- Support two different bus standards: 8080 mode, 6800 mode
- Support 8-bit/16-bit read and write operations
- Controllable transmission speed (up to 10MHz)
- When internal data transmission is enabled or external bus access is completed, DMA transmission can be triggered
- Support DMA read and write

## 5.21 Enhanced serial audio interface（SSIE）

1-channel serial audio interface, which can send and receive audio devices to multiple devices that support different audio data formats:

- Communication mode: master or slave, send and receive (full duplex communication)
- Communication format: I2S format, mono format
- FIFO: 4 bytes * 8 segments transmit or receive FIFO

## 5.22 Quad Serial Peripheral Interface（QSPI）

1-channel Quad Serial Peripheral Interface module (QSPI) is a memory controller for connecting a serial ROM (nonvolatile-memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface.

- Support extended SPI, Dual SPI, Quad SPI protocols
- Configurable to SPI mode 0 and SPI mode 3
- Address width selectable from 8, 16, 24, or 32 bits
- Timing adjustment function to support a wide range of serial flash configurations
- Flash read function for the read, fast read, fast read dual output, fast read dual I/O, fast read quad output, and fast read quad I/O instructions
- Serial flash instructions and functions through software control, including erase, write, ID read, and power-down control

## 5.23 Universal Serial Bus（USB）

1-channel USB module, compatible with USB 2.0 specification, supports host controller mode, device controller mode and OTG function. The host controller supports full-speed and low-speed transmission, and the device controller supports full-speed transmission. The built-in USB transceiver supports control transmission, synchronous transmission, batch transmission and interrupt transmission.

It supports a data transmission FIFO with a maximum of 10 pipes, and pipe 0 is the default DCP pipe. According to peripheral equipment and communication requirements, any endpoint number can be configured to pipes 1~9.

Compatible with USB BC1.2 specification.

## 5.24 Analog-to-digital converter（ADC）

This product has a built-in 12-bit resolution analog-to-digital converter SARADC, which can convert analog input to digital value and supports up to 35 channels of ADC analog input (ANI0～ANI34). The ADC contains the following functions:

- 12-bit resolution, conversion rate 1.42Msps.
- Trigger mode: support software trigger, hardware trigger and hardware trigger in standby state
- Channel selection: support two modes of single-channel selection and multi-channel scanning
- Conversion mode: support single conversion and continuous conversion
- Working voltage: Support the working voltage range of 1.8V≤VDD≤5.5V
- It can detect the built-in reference voltage (1.45V) and temperature sensor.

ADC can set various A/D conversion modes through the following mode combinations.

| | | |
|---|---|---|
| Trigger mode | Software trigger | Start the conversion by software operation. |
| | Hardware trigger no wait mode | Start the conversion by detecting the hardware trigger. |
| | Hardware trigger wait mode | In the conversion standby state with the power off, the power is turned on by detecting the hardware trigger, and the conversion starts automatically after the A/D power stabilization wait time. |
| Channel selection mode | Select mode | Select 1 channel of analog input for A/D conversion. |
| | Scan mode | Perform A/D conversion on 4 channels of analog input in sequence. It is possible to select 4 consecutive channels from ANI0 to ANI15 as analog input. |
| Conversion mode | Single conversion mode | Perform 1 A/D conversion on the selected channel. |
| | Continuous conversion mode | Perform continuous A/D conversion on the selected channel until it is stopped by software. |
| Sampling time/conversion time | Number of sampling clocks/number of conversion clocks | The sampling time can be set by the register. The default value of the sampling clock is 13.5 clk, and the Min value of the conversion clock is 31.5 clk. |

## 5.25 Programmable gain amplifier（PGA）

This product has a built-in programmable gain amplifier (PGA0), which has the following functions:

- Multi-stage gain optional (1/2/4/8/16/32/64/128）
- PGA0 output with sample and hold circuit
- Support offset voltage trimming
- Support single-ended/pseudo-differential input
- Support PGA output test.
- PGA output can be connected to internal analog comparator input for shaping.
- The output of PGA0 can be selected as analog input for A/D converter or analog input for positive terminal of comparator0 (CMP0).
- Support offset voltage software trimming.

## 5.26 Comparator（CMP）

This product has built-in two channels with hysteresis comparatorCMP0 and CMP1, with the following functions:

- Can choose comparator high-speed mode, comparator low-speed mode or comparator window mode.
- Can select external reference voltage input and internal reference voltage for reference voltage.
- The elimination width of the noise elimination digital filter can be selected.
- Can detect the valid edge of the comparator output and generate an interrupt signal.
- It can detect the valid edge of the comparator output and output the event signal to the linkage controller.

## 5.27 Two-wire serial debug port（SW-DP）

ARM's SW-DP interface allows to connect to the microcontroller through a serial wire debugging tool.

## 5.28 Security function

### 5.28.1 Flash CRC calculation function (high-speed CRC, general-purpose CRC)

Detect the data error of flash memory through CRC operation.

According to different purposes and conditions of use, the following 2 CRCs can be used respectively.

- High-speed CRC: In the initialization program, it can stop the operation of the CPU and check the entire code flash area at high speed。
- General CRC: In CPU operation, it is not limited to the code flash area but can be used for multi-purpose checking.

### 5.28.2 RAM Parity error detection function

When reading RAM data, detect parity errors.

### 5.28.3 SFR protection function

Prevent the important SFR (Special Function Register) from being rewritten due to CPU runaway.

### 5.28.4 Illegal memory access detection function

Detect illegal access to illegal memory area (area without memory or area with restricted access).

### 5.28.5 Frequency detection function

Can use timer4 unit to self-check CPU or peripheral hardware clock frequency.

### 5.28.6 A/D test function

Perform A/D conversion on the A/D converter's positive (+) reference voltage, negative (–) reference voltage, analog input channel (ANI), temperature sensor output voltage, and internal reference voltage Self-test.

### 5.28.7 Digital output signal level detection function of input/ output port

When the input/output port is in output mode, the output level of the pin can be read.

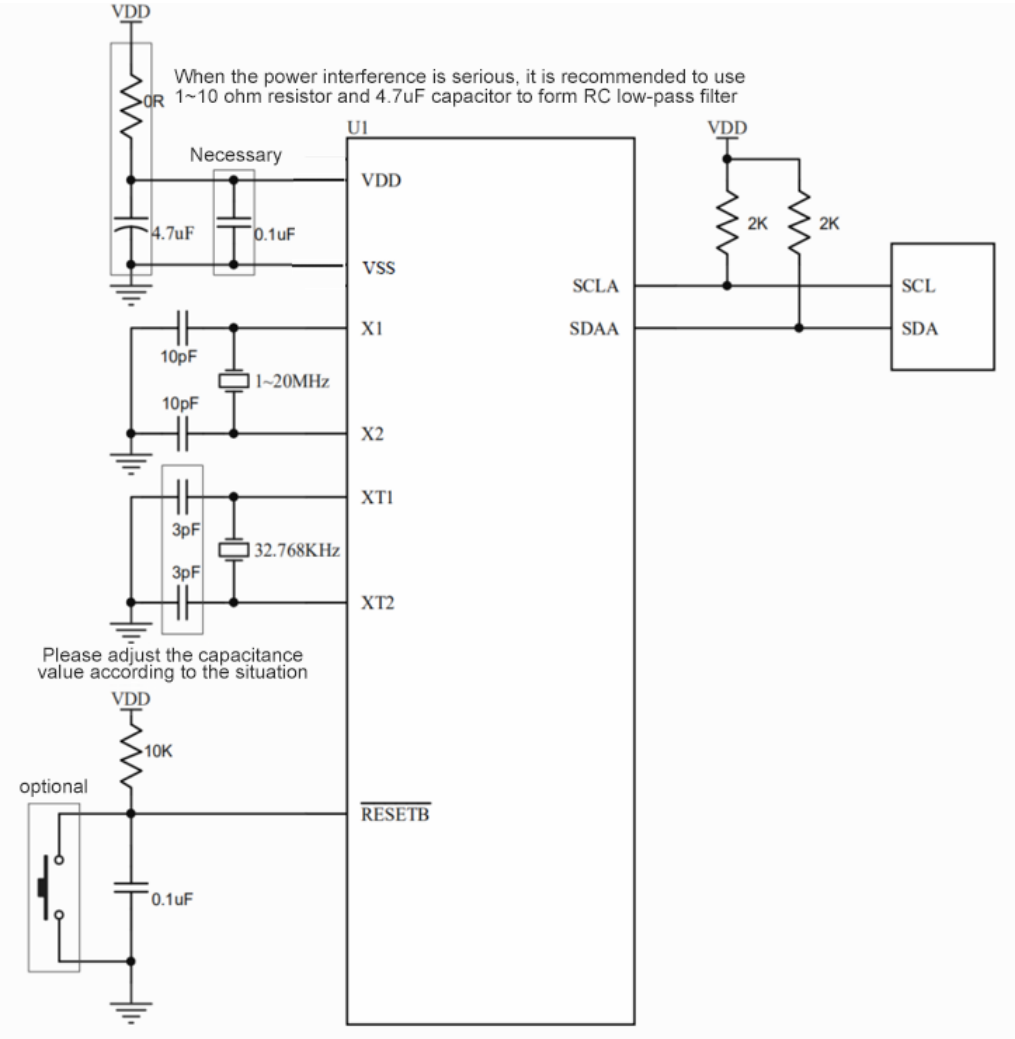
## 5.29 Key function

The input pin (KR0～KR7) can be interrupted by the key to generate a key interrupt (INTKR).

# 6 Electrical characteristics

## 6.1 Typical application peripheral circuit

The device connection reference of the typical MCU application peripheral circuit is as follows:



## 6.2 Absolute maximum voltage rating

（$T_A$=–40～+105℃）

| Item | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Source voltage | VDD | | －0.5～+6.5 | V |
| Input voltage | VI | PA00～PA14、PB00～PB06、PC00～PC15、PD00～PD15、PH00～PH04、EXCLK、EXCLKS、RESETB | －0.3～VDD+0.3 note1 | V |
| Output voltage | VO | PA00～PA14、PB00～PB06、PC00～PC15、PD00～PD15、PH01～PH04 | －0.3～VDD+0.3 note1 | V |
| Analog input voltage | VAI | ANI0～ANI24、ANI27～ANI36 | －0.3～VDD+0.3 and －0.3～AVREF(+)+0.3 note1、2 | V |

Note：1. Do not exceed 6.5V.

2. The pin of the A/D conversion target cannot exceed AVREF(+)+0.3.

Note: Even if one of the items exceeds the absolute maximum rating for an instant, the quality of the product may be degraded. The absolute maximum rating is a rating that may cause physical damage to the product, and the product must be used under the condition that the rating is not exceeded.

Remarks：

1. Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.
2. AVREF(+): The positive (+) reference voltage of the A/D converter
3. Use VSS as the reference voltage.

## 6.3 Absolute maximum current rating

（$T_A$=–40～+105℃）

| Item | Symbol | Condition | | Rating | Unit |
|---|---|---|---|---|---|
| High level output current | IOH1 | Each pin | PA00～PA14、PB00～PB06、PC00～PC15、PD00～PD15、PH01～PH04 | －40 | mA |
| | | Total pins-170mA | PB00～PB06、PD00～PD15 | －70 | mA |
| | | | PA00～PA14、PC00～PC15 | －100 | mA |
| | IOH2 | Each pin | PH01～PH04 | －3 | mA |
| | | Total pins | | －15 | mA |
| Low-level output current | IOL1 | Each pin | PA00～PA14、PB00～PB06、PC00～PC15、PD00～PD15、PH01～PH04 | 40 | mA |
| | | Total pins 170mA | PB00～PB06、PD00～PD15 | 100 | mA |
| | | | PA00～PA14、PC00～PC15 | 120 | mA |
| | IOL2 | Each pin | PH01～PH04 | 15 | mA |
| | | Total pins | | 45 | mA |
| Working temperature | TA | Normally run | | －40～+105 | ℃ |
| | | When flash programming | | | |
| Storage temperature | Tstg | | | －65～+150 | ℃ |

Note: Even if one of the items exceeds the absolute maximum rating for an instant, the quality of the product may be degraded. The absolute maximum rating is a rating that may cause physical damage to the product, and the product must be used under the condition that the rating is not exceeded.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

# 6.4 Oscillation circuit characteristics

## 6.4.1 X1，XT1 characteristics

（$T_A$=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | Resonator | condition | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency (fx) | Ceramic resonator/crystal resonator | 1.8V≤VDD≤5.5V | 1.0 | - | 20.0 | MHz |
| XT1 clock oscillation frequency (fxt) | Crystal resonator | 1.8V≤VDD≤5.5V | 32 | 32.768 | 35 | kHz |

Note：

1. It only indicates the allowable frequency range of the oscillation circuit. Please refer to the AC characteristics for the command execution time.
2. Please entrust the resonator manufacturer to evaluate after installing the circuit, and use it after confirming the oscillation characteristics.

## 6.4.2 Internal oscillator characteristics

（$T_A$=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| resonator | condition | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|
| High-speed internal oscillator clock frequency (fIH)note1,2 | | 1.0 | | 64.0 | MHz |
| Clock frequency accuracy of high-speed internal oscillator | $T_A$ = +10 ～ +70℃ | -1.0 | | +1.0 | % |
| | $T_A$ = -10 ～ +105℃ | -1.5note3 | | +1.5note3 | % |
| | $T_A$ = -40 ～ +105℃ | -4.0note3 | | +4.0note3 | % |
| Clock frequency of low-speed internal oscillator (fIL) | | 10 | 15 | 20 | kHz |

Note：

1. Select the frequency of the high-speed internal oscillator by the option byte.
2. It only shows the characteristics of the oscillation circuit, please refer to the AC characteristics for the command execution time.
3. Low temperature specification value is guaranteed by design, mass production does not measure low temperature condition.

## 6.4.3 PLL oscillator characteristics

（TA=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| resonator | condition | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|
| PLL input frequency note1 | | 4.0 | | 8.0 | MHz |
| PLL lock time | | 40 | | | μs |
| UPLL input frequency | | 4.0 | | 8.0 | MHz |
| UPLL lock time | | 40 | | | μs |

Note：1. It only shows the characteristics of the oscillation circuit, please refer to the AC characteristics for the command execution time

# 6.5 DC characteristics

## 6.5.1 Pin characteristics

（TA=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | symbol | condition | | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|---|---|
| high leveloutput Current note1 | IOH1 | PA00～PA14、PB00～PB06、PC00～PC15、PD00～PD15 1 pin alone | 1.8V≤VDD≤5.5V –40～+85℃ | | | -12.0note2 | mA |
| | | | 1.8V≤VDD≤5.5V 85～+105℃ | | | -6.0note2 | |
| | | PB00～PB06、PD00～PD15 Total pins (when duty cycle ≤70%note3) | 4.0V≤VDD≤5.5V –40～+85℃ | | | -60.0 | mA |
| | | | 4.0V≤VDD≤5.5V 85～+105℃ | | | -30.0 | |
| | | | 2.4V≤VDD＜4.0V | | | -12.0 | mA |
| | | | 1.8V≤VDD＜2.4V | | | -6.0 | mA |
| | | PA00～PA14、PC00～PC15 Total pins (when duty cycle ≤70%note3) | 4.0V≤VDD≤5.5V –40～+85℃ | | | -80.0 | mA |
| | | | 4.0V≤VDD≤5.5V 85～+105℃ | | | -30.0 | |
| | | | 2.4V≤VDD＜4.0V | | | -20.0 | mA |
| | | | 1.8V≤VDD＜2.4V | | | -10.0 | mA |
| | | Total pins (when duty cycle ≤70%note3) | 1.8V≤VDD≤5.5V –40～+85℃ | | | -140.0 | mA |
| | | | 1.8V≤VDD≤5.5V 85～+105℃ | | | -60.0 | |
| | IOH2 | PH01～PH04 1 pin alone | 1.8V≤VDD≤5.5V | | | -2.5note2 | mA |
| | | Total pins (when duty cycle ≤70%note3) | 1.8V≤VDD≤5.5V | | | -10 | mA |

Note：

1. This is the current value that guarantees the operation of the device even if current flows from the VDD pin to the output pin。

2. Can not exceed the total current value。

3. This is the output current value of "duty cycle≤70%condition"。

To change the output current value with a duty cycle> 70% can be calculated with the following calculation formula (when the duty cycle is changed to n%).

• The total output current of the pins = (IOH×0.7)/(n×0.01)

＜example＞ IOH =–10.0mA、n =80%

The total output current of the pins = (–10.0×0.7)/(80×0.01) ≈ –8.7mA

The current of each pin does not change due to the duty cycle, and no current above the absolute maximum rating will flow.

Remark: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

（$T_A$=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | symbol | condition | | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|---|---|
| Low-level output current[note 1] | IOL1 | PA00～PA14、PB00～PB06、PC00～PC15、PD00～PD15 1 pin alone | 1.8V≤VDD≤5.5V –40～+85℃ | | | 35[note 2] | mA |
| | | | 1.8V≤VDD≤5.5V 85～+105℃ | | | 20[note 2] | mA |
| | | PB00～PB06、PD00～PD15 Total pins (when duty cycle ≤70%[note3]) | 4.0V≤VDD≤5.5V –40～+85℃ | | | 100 | mA |
| | | | 4.0V≤VDD≤5.5V 85～+105℃ | | | 70 | mA |
| | | | 2.4V≤VDD＜4.0V | | | 30 | mA |
| | | | 1.8V≤VDD＜2.4V | | | 15 | mA |
| | | PA00～PA14、PC00～PC15 Total pins (when duty cycle ≤70%[note3]) | 4.0V≤VDD≤5.5V –40～+85℃ | | | 120 | mA |
| | | | 4.0V≤VDD≤5.5V 85～+105℃ | | | 80 | mA |
| | | | 2.4V≤VDD＜4.0V | | | 40 | mA |
| | | | 1.8V≤VDD＜2.4V | | | 20 | mA |
| | | Total pins (when duty cycle ≤70%[note3]) | 1.8V≤VDD≤5.5V –40～+85℃ | | | 150 | mA |
| | | | 1.8V≤VDD≤5.5V 85～+105℃ | | | 100 | mA |
| | IOL2 | PH01～PH04 1 pin alone | 1.8V≤VDD≤5.5V | | | 10[note 2] | mA |
| | | Total pins (when duty cycle ≤70%[note3]) | 1.8V≤VDD≤5.5V | | | 40 | mA |

Note:

1. This is the current value that guarantees the operation of the device even if the current flows from the output pin to the VSS pin.

2. Can not exceed the total current value.

3. This is the output current value of "duty cycle≤70% condition"。

The output current value with a duty cycle> 70% can be calculated with the following calculation formula (when the duty cycle is changed to n%）

• The total output current of the pins = (IOL×0.7)/(n×0.01)

＜example＞ IOL= 10.0mA、n = 80%

The total output current of the pins = (10.0×0.7)/(80×0.01) ≈ 8.7mA

The current of each pin does not change due to the duty cycle, and no current above the absolute maximum rating will flow.

Remark：Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

（$T_A$=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | symbol | condition | | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|---|---|
| High level input voltage | VIH1 | PA00～PA14、PB00～PB06、PC00～PC15、PD00～PD15、PH00～PH04、EXCLK、EXCLKS、RESETB | Schmidt input | 0.8VDD | | VDD | V |
| Low-level input voltage | VIL1 | PA00～PA14、PB00～PB06、PC00～PC15、PD00～PD15、PH00～PH04、EXCLK、EXCLKS、RESETB | Schmidt input | 0 | | 0.2VDD | V |

Note: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

（$T_A$=–40 ～ +105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | symbol | condition | | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|---|---|
| High level output voltage | VOH1 | PA00～PA14、PB00～PB06、PC00～PC15、PD00～PD15 | 4.0V≤VDD≤5.5V、IOH1= - 12.0mA | VDD - 1.5 | | | V |
| | | | 4.0V≤VDD≤5.5V、IOH1= - 6.0mA | VDD - 0.7 | | | V |
| | | | 2.4V≤VDD≤5.5V、IOH1= - 3.0mA | VDD - 0.6 | | | V |
| | | | 1.8V≤VDD≤5.5V、IOH1= - 2mA | VDD - 0.5 | | | V |
| | VOH2 | PH01～04 | 4.0V≤VDD≤5.5V、IOH2= - 2.5mA | VDD - 1.5 | | | V |
| | | | 4.0V≤VDD≤5.5V、IOH2= - 1.5mA | VDD - 0.7 | | | V |
| | | | 2.4V≤VDD≤5.5V、IOH2= - 0.5mA | VDD - 0.6 | | | V |
| | | | 1.8V≤VDD≤5.5V、IOH2= - 0.4mA | VDD - 0.5 | | | V |
| Low-level output voltage | VOL1 | PA00～PA14、PB00～PB06、PC00～PC15、PD00～PD15 | 4.0V≤VDD≤5.5V、IOL1=35.0mA | | | 1.2 | V |
| | | | 4.0V≤VDD≤5.5V、IOL1=20.0mA | | | 0.7 | V |
| | | | 2.4V≤VDD≤5.5V、IOL1=9.0mA | | | 0.4 | V |
| | | | 1.8V≤VDD≤5.5V、IOL1=6.0mA | | | 0.4 | V |
| | VOL2 | PH01～04 | 4.0V≤VDD≤5.5V、IOL2=10.0mA | | | 1.2 | V |
| | | | 4.0V≤VDD≤5.5V、IOL2=6.0mA | | | 0.7 | V |
| | | | 2.4V≤VDD≤5.5V、IOL2=2.5mA | | | 0.4 | V |
| | | | 1.8V≤VDD≤5.5V、IOL2=1.5mA | | | 0.4 | V |

Note: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins

（$T_A$=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | symbol | condition | | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|---|---|
| High-level input leakage current | ILIH1 | PA00～PA14、PB00～PB06、PC00～PC15、PD00～PD15、PH00 | VI=VDD | | | 1 | μA |
| | ILIH2 | RESETB | VI=VDD | | | 1 | μA |
| | ILIH3 | PH01～04 （X1、X2、EXCLK、XT1、XT2、EXCLKS） | VI=VDD, when input port and external clock input | | | 1 | μA |
| | | | VI=VDD, when the resonator is connected | | | 10 | μA |
| Low-level input leakage current | ILIL1 | PA00～PA14、PB00～PB06、PC00～PC15、PD00～PD15、PH00 | VI=VSS | | | -1 | μA |
| | ILIL2 | RESETB | VI=VSS | | | -1 | μA |
| | ILIL3 | PH01～04 （X1、X2、EXCLK、XT1、XT2、EXCLKS） | VI=VSS, when input port and external clock input | | | -1 | μA |
| | | | VI=VSS, when the resonator is connected | | | -10 | μA |
| Internal pull-up resistor | RU | PA00～PA06、PA10～PA14、PB00～PB06、PC00～PC15、PD00～PD15、PH00～PH02 | VI=VSS, when input port | 10 | 30 | 100 | KΩ |
| Internal pull-down resistor | RD | PA00～PA06、PA09～PA14、PB00～PB06、PC00～PC15、PD00～PD15 | VI=VDD, when input port | 10 | 30 | 100 | KΩ |

Note: Unless otherwise specified, the characteristics of multiplexed pins are the same as those of port pins.

## 6.5.2 Power supply current characteristics

（$T_A$=–40～+105℃、1.8V≤VDD≤5.5V、$V_{SS}$=0V）

| item | symbol | condition | | | MIN. | TYP. | MAX. | unit |
|---|---|---|---|---|---|---|---|---|
| current note1 | $I_{DD1}$ | Operating mode | High-speed internal oscillator | $f_{HOCO}$=64MHz、$f_{IH}$=64MHz note2 | | 7.6 | 12.5 | mA |
| | | | | $f_{HOCO}$=32MHz、$f_{IH}$=32MHz note2 | | 5.8 | 7.8 | |
| | | | High-speed main system clock | $f_{MX}$=20MHz note3 Input square wave | | 4.0 | 5.2 | mA |
| | | | | Connect the crystal | | 4.0 | 5.2 | |
| | | | Subsystem clock operation | $f_{SUB}$=32.768kHz note4 Input square wave | | 70 | 85 | uA |
| | | | | Connect the crystal | | 70 | 85 | |
| | | | Low-speed internal oscillator | fIL=15kHz note8 | | 70 | 85 | uA |
| | $I_{DD2}$ | Sleep mode | High-speed internal oscillator | $f_{HOCO}$=64MHz、$f_{IH}$=64MHz note2 | | 1.8 | 7.0 | mA |
| | | | | $f_{HOCO}$=32MHz、$f_{IH}$=32MHz note2 | | 1.2 | 3.8 | |
| | | | High-speed main system clock | $f_{MX}$=20MHz note3 Input square wave | | 0.7 | 2.5 | mA |
| | | | | Connecting crystal | | 0.7 | 2.5 | |
| | | | Subsystem clock operation | $f_{SUB}$=32.768kHz note5 Input square wave | | 1.2 | 14.5 | uA |
| | | | | Connecting crystal | | 1.2 | 14.5 | |
| | | | Low-speed internal oscillator | fIL=15kHz note8 | | 1.4 | 15 | uA |
| | $I_{DD3}$ note6 | Deep sleep mode note 7 | $T_A$=–40℃~+70℃ VDD=3.0V | | | 0.7 | 1.5 | uA |
| | | | $T_A$=–40℃~+85℃ VDD=3.0V | | | 0.7 | 11.5 | |
| | | | $T_A$=–40℃~+105℃ VDD=3.0V | | | 0.7 | 14.5 | |

Note：

1) This is the current flowing through VDD, including the input leakage current when the input pin is fixed to VDD or VSS. TYP. Value: CPU is in the execution of multiplication instruction (IDD1)，and does not include peripheral operating current. MAX. Value: CPU is in full instruction execution action (IDD1), and includes peripheral operating current, but does not include the flow to the A/D converter、The current of the LVD circuit, I/O port, and internal pull-up or pull-down resistors does not include the current when rewriting data flash memory.
2) This is the case when the high-speed internal oscillator and the subsystem clock stop oscillating.
3) This is the case where the high-speed main system clock and subsystem clock stop oscillating.
4) This is the case when the high-speed internal oscillator and the high-speed main system clock stop oscillating.
5) This is the case when the high-speed internal oscillator and the high-speed main system clock stop oscillating. Contains the current flowing to the RTC, but does not include the 15-bit interval timer and watchdog timer current.

6) Does not include current to RTC, 15-bit interval timer and watchdog timer.

7) For the current value when the subsystem clock is running in the deep sleep mode, please refer to the current value when the subsystem clock is running in the sleep mode.

8) This is the case where the high-speed internal oscillator, the high-speed main system clock and the subsystem clock stop oscillating.

Note：

1) $f_{HOCO}$ : The clock frequency of the high-speed internal oscillator, fIH: the system clock frequency provided by the high-speed internal oscillator。

2) $f_{SUB}$ ： External subsystem clock frequency (XT1/XT2 clock oscillation frequency).

3) $f_{MX}$ ： External main system clock frequency (X1/X2 clock oscillation frequency).

4) $f_{IL}$ ： Clock frequency of low-speed internal oscillator.

5) TYP. The temperature condition of the value is TA=25°C.

（$T_A$=–40～+105℃、1.8V≤VDD≤5.5V、$V_{SS}$=0V）

| parameter | symbol | condition | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed internal oscillator operating current | IFIL note1 | | | | 0.2 | | uA |
| RTC operating current | IRTC note1,2,3 | | | | 0.04 | | uA |
| 15-bit interval timer operating current | IIT note1,2,4 | | | | 0.02 | | uA |
| Watchdog timer operating current | IWDT note1,2,5 | fIL=15kHz | | | 0.22 | | uA |
| A/D converter operating current | IADC note1,6 | ADC HS mode@64MHz | | | 2.2 | | mA |
| | | ADC HS mode@4MHz | | | 1.3 | | mA |
| | | ADC LC mode@24MHz | | | 1.1 | | mA |
| | | ADC LC mode@4MHz | | | 0.8 | | mA |
| PGA operating current | IPGA note1,7 | Each channel | | | 480 | 700 | uA |
| comparator operating current | ICMP note1,8 | Each channel | Does not use internal reference voltage | | 60 | 100 | uA |
| | | | Use internal reference voltage | | 80 | 140 | uA |
| LVD operating current | ILVD note1,9 | | | | 0.08 | | uA |

note：

1) This is the current flowing through VDD.
2) This is the case when the high-speed internal oscillator and the high-speed system clock stop oscillating。
3) This is the current that only flows to the real-time clock (RTC) (not including the operating current of the low-speed internal oscillator and XT1 oscillator circuit). When the real-time clock is running in running mode or sleep mode, the current value of the microcontroller is IDD1 or IDD2 plus the value of IRTC. In addition, when low-speed internal oscillator is selected, IFIL must be added. IDD2 when the subsystem clock is running contains the operating current of the real-time clock.
4) This is the current that only flows to the 15-bit interval timer (not including the operating current of the low-speed internal oscillator and XT1 oscillator circuit). When the 15-bit interval timer is running in run mode or sleep mode, the current value of the microcontroller is the value of IDD1 or IDD2 plus IIT. In addition, when low-speed internal oscillator is selected, IFIL must be added.
5) This is the current that only flows to the watchdog timer (including the operating current of the low-speed internal oscillator). When the watchdog timer is running, the current value of the microcontroller is IDD1 or IDD2 or IDD3 plus the value of IWDT.
6) This is the current that only flows to the A/D converter. When the A/D converter is running in running mode or sleep mode, the current value of the microcontroller is IDD1 or IDD2 plus the value of IADC.
7) This is the current that only flows to the PGA circuit. When the programmable gain amplifier circuit is running, the current value of the microcontroller is the value of IDD1 or IDD2 or IDD3 plus IPGA.
8) This is the current that only flows to the comparator circuit. When the comparator circuit is running, the current value of the microcontroller is the value of IDD1 or IDD2 or IDD3 plus ICMP.
9) This is the current that only flows to the LVD circuit. In the case of LVD circuit operation, the current value of the microcontroller is the value of IDD1 or IDD2 or IDD3 plus ILVD.

Note：

1) $f_{IL}$ ： Clock frequency of low-speed internal oscillator.
2) TYP. The temperature condition of the value is TA=25℃。

## 6.6 AC characteristic

（TA=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | symbol | condition | | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|---|---|
| Instruction cycle (Minimum instruction execution time) | TCY | The main system clock (fMAIN) runs | 1.8V≤VDD≤5.5V | 0.015625 | | 1 | μs |
| | | Subsystem clock (fSUB) operation | 1.8V≤VDD≤5.5V | 28.5 | 30.5 | 31.3 | μs |
| External system clock frequency | fEX | 1.8V≤VDD≤5.5V | | 1.0 | | 20.0 | MHz |
| | fEXS | 1.8V≤VDD≤5.5V | | 32.0 | | 35.0 | kHz |
| High and low level width of external system clock input | tEXH、tEXL | 1.8V≤VDD≤5.5V | | 24 | | | ns |
| | tEXHS、tEXLS | 1.8V≤VDD≤5.5V | | 13.7 | | | μs |
| TI00 ～TI03, TI10 ～ TI13, input high and low level width | tTIH、tTIL | 1.8V≤VDD≤5.5V | | 1/fMCK+10 | | | ns |
| TO00 ～ TO03, TO10 ～ TO13, output frequency | fTO | 4.0V≤VDD≤5.5V | | | | 16 | MHz |
| | | 2.4V≤VDD＜4.0V | | | | 8 | MHz |
| | | 1.8V≤VDD＜2.4V | | | | 4 | MHz |
| CLKBUZ0, CLKBUZ1 Output frequency | fPCL | 4.0V≤VDD≤5.5V | | | | 16 | MHz |
| | | 2.4V≤VDD＜4.0V | | | | 8 | MHz |
| | | 1.8V≤VDD＜2.4V | | | | 4 | MHz |
| Interrupt input high and low level width | tINTH、tINTL | INTP0 ～ INTP3 | 1.8V≤VDD≤5.5V | 1 | | | μs |
| Key interrupt input high and low level width | tKR | KR0 ～ KR5 | 1.8V≤VDD≤5.5V | 250 | | | ns |
| RESETB low-level width | tRSL | | | 10 | | | μs |

Note：fMCK：Operating clock frequency of timer4 unit。

# 6.7 Peripheral features

## 6.7.1 Universal interface unit

1) UART mode

- （$T_A$=–40～+85℃、1.8V≤VDD≤5.5V、$V_{SS}$=0V）

| item | condition | | Specification Value | | unit |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| Transfer rate | 1.8V ≤ VDD ≤ 5.5V | | | fMCK/6 | bps |
| | | The theoretical value of the maximum transfer rate fMCK=fCLK | | 10.6 | Mbps |

- （$T_A$=+85～+105℃、1.8V≤VDD≤5.5V、$V_{SS}$=0V）

| item | condition | | Specification Value | | unit |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| Transfer rate | 1.8V ≤ VDD ≤ 5.5V | | | fMCK/12 | bps |
| | | Theoretical value of the maximum transfer rate fMCK=fCLK | | 5.3 | Mbps |

2) Three-wire SPImode (master mode, internal clock output)

（$T_A$=–40～+105℃、1.8V≤VDD≤5.5V、$V_{SS}$=0V）

| item | symbol | condition | | –40 ～ +85℃ | | +85 ～ +105℃ | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| SCLKp cycle time | tKCY1 | tKCY1 ≥ 2/fCLK | 4.0V ≤ VDD ≤ 5.5V | 31.25 | | 62.5 | | ns |
| | | | 2.7V ≤ VDD ≤ 5.5V | 41.67 | | 83.33 | | ns |
| | | | 2.4V ≤ VDD ≤ 5.5V | 65 | | 125 | | ns |
| | | | 1.8V ≤ VDD ≤ 5.5V | 125 | | 250 | | ns |
| SCLKp high/low level width | tKH1、tKL1 | 4.0V ≤ VDD ≤ 5.5V | | tKCY1/2–4 | | tKCY1/2–7 | | ns |
| | | 2.7V ≤ VDD ≤ 5.5V | | tKCY1/2–5 | | tKCY1/2–10 | | ns |
| | | 2.4V ≤ VDD ≤ 5.5V | | tKCY1/2–10 | | tKCY1/2–20 | | ns |
| | | 1.8V ≤ VDD ≤ 5.5V | | tKCY1/2–19 | | tKCY1/2–38 | | ns |
| SDIp preparation time (to SCLKp↑) | tSIK1 | 4.0V ≤ VDD ≤ 5.5V | | 12 | | 23 | | ns |
| | | 2.7V ≤ VDD ≤ 5.5V | | 17 | | 33 | | ns |
| | | 2.4V ≤ VDD ≤ 5.5V | | 20 | | 38 | | ns |
| | | 1.8V ≤ VDD ≤ 5.5V | | 28 | | 55 | | ns |
| SDIp hold time (to SCLKp↑) | tKSI1 | 1.8V ≤ VDD ≤ 5.5V | | 5 | | 10 | | ns |
| SCLKp↓→SDOp output delay time | tKSO1 | 1.8V ≤ VDD ≤ 5.5V C=20pF note1 | | | 5 | | 10 | ns |

note1.：C is the load capacitance of the SCLKp and SDOp output lines。

note：Through the port inputmode register and the port outputmode register, the SDIp pin is selected as the normal input buffer and theSDOp the pin and SCLKp pin are selected as the usual output mode。

3) Three-wire SPImode (slave mode, external clock input)

（TA=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | symbol | condition | | –40 ～ +85℃ | | +85 ～ +105℃ | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| SCLKp cycle time | tKCY2 | 4.0V ≤ VDD ≤ 5.5V | 20MHz < fMCK | 8/fMCK | | 16/fMCK | | ns |
| | | | fMCK ≤20MHz | 6/fMCK | | 12/fMCK | | ns |
| | | 2.7V ≤ VDD ≤ 5.5V | 16MHz < fMCK | 8/fMCK | | 16/fMCK | | ns |
| | | | fMCK ≤16MHz | 6/fMCK | | 12/fMCK | | ns |
| | | 2.4V ≤ VDD ≤ 5.5V | | 6/fMCK and 500 | | 12/fMCK and 1000 | | ns |
| | | 1.8V ≤ VDD ≤ 5.5V | | 6/fMCK and 750 | | 12/fMCK and 1500 | | ns |
| SCLKp high/low level width | tKH2、tKL2 | 4.0V ≤ VDD ≤ 5.5V | | tKCY1/2–7 | | tKCY1/2–14 | | ns |
| | | 2.7V ≤ VDD ≤ 5.5V | | tKCY1/2–8 | | tKCY1/2–16 | | ns |
| | | 1.8V ≤ VDD ≤ 5.5V | | tKCY1/2–18 | | tKCY1/2–36 | | ns |
| SDIp preparation time (To SCLKp↑) | tSIK2 | 2.7V ≤ VDD ≤ 5.5V | | 1/fMCK+20 | | 1/fMCK+40 | | ns |
| | | 1.8V ≤ VDD ≤ 5.5V | | 1/fMCK+30 | | 1/fMCK+60 | | ns |
| SDIp hold time (To SCLKp↑) | tKSI2 | 1.8V ≤ VDD ≤ 5.5V | | 1/fMCK+31 | | 1/fMCK+62 | | ns |
| SCLKp↓→SDOp output delay time | tKSO2 | 2.7V ≤ VDD ≤ 5.5V C=30pF note1 | | | 2/fMCK+44 | | 2/fMCK+66 | ns |
| | | 2.4V ≤ VDD ≤ 5.5V C=30pF note1 | | | 2/fMCK+75 | | 2/fMCK+113 | ns |
| | | 1.8V ≤ VDD ≤ 5.5V C=30pF note1 | | | 2/fMCK+100 | | 2/fMCK+150 | ns |

note1：C is the load capacitance of the SCLKp and SDOp output lines.

note：Through the port inputmode register and the port outputmode register, select the SDIp pin and SCLKp pin as the normal input buffer and select the SDOp pin as the normal output mode.

4) Four-wire SPI mode (slave mode, external clock input)

（TA=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | symbol | condition | | –40 ～ +85℃ | | +85 ～ +105℃ | | unit |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| SSI00 set up time | tSSIK | DAPmn=0 | 2.7V ≤ VDD ≤ 5.5V | 120 | | 240 | | ns |
| | | | 1.8V ≤ VDD ≤ 5.5V | 200 | | 400 | | ns |
| | | DAPmn=1 | 2.7V ≤ VDD ≤ 5.5V | 1/fMCK+120 | | 1/fMCK+240 | | ns |
| | | | 1.8V ≤ VDD ≤ 5.5V | 1/fMCK+200 | | 1/fMCK+400 | | ns |
| SSI00 hold time | tKSSI | DAPmn=0 | 2.7V ≤ VDD ≤ 5.5V | 1/fMCK+120 | | 1/fMCK+240 | | ns |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 1.8V ≤ VDD ≤ 5.5V | 1/fMCK+200 | | 1/fMCK+400 | | ns |
| | | DAPmn=1 | 2.7V ≤ VDD ≤ 5.5V | 120 | | 240 | | ns |
| | | | 1.8V ≤ VDD ≤ 5.5V | 200 | | 400 | | ns |

note：Through the port inputmode register and the port outputmode register, select the SDIp pin and SCLKp pin as the normal input buffer and select the SDOp pin as the normal outputmode.

5) Simple IIC mode

（$T_A$=–40～+105℃、1.8V≤VDD≤5.5V、$V_{SS}$=0V）

| item | symbol | condition | –40 ～ +85℃ | | +85 ～ +105℃ | | unit |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| SCLr Clock frequency | fSCL | 2.7V ≤ VDD ≤ 5.5V<br>Cb = 50 pF, Rb = 2.7 kΩ | | 1000note1 | | 400note1 | kHz |
| | | 1.8V ≤ VDD ≤ 5.5V<br>Cb = 100 pF, Rb = 3 kΩ | | 400note1 | | 100note1 | kHz |
| | | 1.8V ≤ VDD ≤ 2.7V<br>Cb = 100 pF, Rb = 5 kΩ | | 300note1 | | 75note1 | kHz |
| Hold time when SCLr is low | tLOW | 2.7V ≤ VDD ≤ 5.5V<br>Cb = 50 pF, Rb = 2.7 kΩ | 475 | | 1200 | | ns |
| | | 1.8V ≤ VDD ≤ 5.5V<br>Cb = 100 pF, Rb = 3 kΩ | 1150 | | 4600 | | ns |
| | | 1.8V ≤ VDD ≤ 2.7V<br>Cb = 100 pF, Rb = 5 kΩ | 1550 | | 6500 | | ns |
| Hold time when SCLr is high | tHIGH | 2.7V ≤ VDD ≤ 5.5V<br>Cb = 50 pF, Rb = 2.7 kΩ | 475 | | 1200 | | ns |
| | | 1.8V ≤ VDD ≤ 5.5V<br>Cb = 100 pF, Rb = 3 kΩ | 1150 | | 4600 | | ns |
| | | 1.8V ≤ VDD ≤ 2.7V<br>Cb = 100 pF, Rb = 5 kΩ | 1550 | | 6500 | | ns |
| Data establishment time (received) | tSU：DAT | 2.7V ≤ VDD ≤ 5.5V<br>Cb = 50 pF, Rb = 2.7 kΩ | 1/fMCK+85note2 | | 1/fMCK+220note2 | | ns |
| | | 1.8V ≤ VDD ≤ 5.5V<br>Cb = 100 pF, Rb = 3 kΩ | 1/fMCK+145note2 | | 1/fMCK+580note2 | | ns |
| | | 1.8V ≤ VDD ≤ 2.7V<br>Cb = 100 pF, Rb = 5 kΩ | 1/fMCK+230note2 | | 1/fMCK+1200note2 | | ns |
| Data retention time (send) | tHD：DAT | 2.7V ≤ VDD ≤ 5.5V<br>Cb = 50 pF, Rb = 2.7 kΩ | | 305 | | 770 | ns |
| | | 1.8V ≤ VDD ≤ 5.5V<br>Cb = 100 pF, Rb = 3 kΩ | | 355 | | 1420 | ns |
| | | 1.8V ≤ VDD ≤ 2.7V<br>Cb = 100 pF, Rb = 5 kΩ | | 405 | | 2070 | ns |

note：1. Must be set to at least fMCK/4.

2. The set value of fMCK cannot exceed the holding time of SCLr="L" and SCLr="H".

## 6.7.2 Serial interface IICA

1) I2C standard mode

（TA=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | symbol | condition | Specification Value | | unit |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| SCLA0 clock frequency | fSCL | Standard mode：fCLK≥1MHz | | 100 | kHz |
| Start condition set up time | tSU：STA | | 4.7 | | μs |
| Start condition hold time note1 | tHD：STA | | 4.0 | | μs |
| Hold time when SCLA0 is low | tLOW | | 4.7 | | μs |
| Hold time when SCLA0 is high | tHIGH | | 4.0 | | μs |
| Data establishment time (received) | tSU：DAT | | 250 | | ns |
| Data retention time (send)note2 | tHD：DAT | | 0 | 3.45 | μs |
| Stop condition set up time | tSU：STO | | 4.0 | | μs |
| Bus idle time | tBUF | | 4.7 | | μs |

note：

a) Generate the first clock pulse after generating the start condition or restarting the condition.

b) During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK).

Note：

The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Standard mode: Cb=400pF, Rb=2.7kΩ

2) I2C fast mode

（TA=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | symbol | condition | Specification Value | | unit |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| SCLA0 clock frequency | fSCL | Fast mode：fCLK≥3.5MHz | | 400 | kHz |
| Start condition set up time | tSU：STA | | 0.6 | | μs |
| Start condition hold time note1 | tHD：STA | | 0.6 | | μs |
| Hold when SCLA0 is low time | tLOW | | 1.3 | | μs |

| | | | | | |
|---|---|---|---|---|---|
| Hold when SCLA0 is high time | tHIGH | | 0.6 | | μs |
| Data set up time (received) | tSU：DAT | | 100 | | ns |
| Data hold time (send)note2 | tHD：DAT | | 0 | 0.9 | μs |
| Stop condition set up time | tSU：STO | | 0.6 | | μs |
| Bus idle time | tBUF | | 1.3 | | μs |

note：

a) Generate the first clock pulse after generating the start condition or restarting the condition.

b) During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK)。

Note：The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Fast mode: Cb=320pF, Rb=1.1kΩ

3) I2C enhanced fast mode

（TA=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | symbol | condition | Specification Value | | unit |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| SCLA0 clock frequency | fSCL | Enhanced fast mode：fCLK≥10MHz | | 1000 | kHz |
| Start condition set up time | tSU：STA | | 0.26 | | μs |
| Start condition hold time note1 | tHD：STA | | 0.26 | | μs |
| Hold time when SCLA0 is low | tLOW | | 0.5 | | μs |
| When SCLA0 is high hold time | tHIGH | | 0.26 | | μs |
| Data set up time (received) | tSU：DAT | | 50 | | ns |
| Data hold time (send)note2 | tHD：DAT | | 0 | 0.45 | μs |
| Stop condition set up time | tSU：STO | | 0.26 | | μs |
| Bus idle time | tBUF | | 0.5 | | μs |

note：

a) Generate the first clock pulse after generating the start condition or restarting the condition.

b) During normal transmission, tHD: the maximum value of DAT (MAX.) needs to be guaranteed, and it is necessary to wait for an acknowledgement (ACK).

Note：The MAX. value of Cb (communication line capacitance) of each mode and the value of Rb (communication line pull-up resistance value) at this time are as follows:

Enhanced fast mode: Cb=120pF, Rb=1.1Kω

## 6.7.3 USB unit characteristics

1) USB characteristic

（VCC = VCC_USB = 3.0 to 3.6 V, Ta = -20 to +85℃ (USBCLKSEL = 1),
Ta = -40 to +105℃ (USBCLKSEL = 0)）

| item | | | symbol | Specification Value | | unit | condition |
|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | | |
| Input characteristic | inputhigh level | | VIH | 2.0 | - | V | - |
| | inputlow level | | VIL | - | 0.8 | V | - |
| | Differential input sensitivity | | VDI | 0.2 | - | V | DP - DM |
| | Differential common mode range | | VCM | 0.8 | 2.5 | V | - |
| Output characteristic | outputhigh level | | VOH | 2.8 | VCC_USB | V | |
| | outputlow level | | VOL | 0.0 | 0.3 | V | |
| | Crossover voltage | | VCRS | | | V | |
| | Rise Time | FS | tr | | | ns | |
| | | LS | | | | | |
| | Fall time | FS | tf | | | ns | |
| | | LS | | | | | |
| | Rise and fall time ratio | FS | tr/tf | | | % | |
| | | LS | | | | | |
| | output resistance | | ZDRV | | | Ω | |
| VBUS | VBUS input voltage | | VIH | VCC x 0.8 | - | V | |
| | | | VIL | - | VCC x 0.2 | V | |
| Pull up pull down | Pull-up resistor | | RPD | | | Ω | |
| | Pull-down resistor | | RPUI | | | Ω | |
| | | | RPUA | | | Ω | |
| Charging batteries specification | D+ leakage current | | IDP_SINK | | | μA | |
| | D-Leakage current | | IDM_SINK | | | μA | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | DCD source current | IDP_SRC | | | μA | |
| | Data detection voltage | VDAT_REF | 0.25 | 0.4 | V | |
| | D+ source voltage | VDP_SRC | 0.5 | 0.7 | V | |
| | D-source voltage | VDM_SRC | 0.5 | 0.7 | V | |

2) USB external power supply

| item | Specification Value | | | unit | condition |
|---|---|---|---|---|---|
| | MIN | TYP | MAX | | |
| UVDD supply current | - | | 50 | mA | |
| UVDD supply voltage | 3.0 | - | 3.6 | V | |

# 6.8 Analog characteristic

## 6.8.1 A/D converter characteristic

The distinction of A/D converter characteristic

| Input channel \ Reference voltage | Reference voltage (+)=AVREFP<br>Reference voltage (--)=AVREFM | Reference voltage (+)=VDD<br>Reference voltage (--)=VSS |
|---|---|---|
| ANI0～ANI34 | See 6.7.1(1)。 | See (2)。 |
| Internal reference voltage, output voltage of temperature sensor | | |

1) Select the case of reference voltage (+)=AVREFP/ANI2, reference voltage (–)=AVREFM/ANI3

(TA=-40～+105℃, 1.8V≤AVREFP≤VDD≤5.5V, VSS=0V, reference voltage (+)=AVREFP, reference voltage (–)=AVREFM=0V)

| item | symbol | condition | | MIN. | TYP. | MAX. | unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | 12 | | bit |
| Composite error note 1 | AINL | 12-bit resolution | 1.8V ≤$AV_{REFP}$ ≤5.5V | | 3 | | LSB |
| Conversion time note 3 | $t_{CONV}$ | 12-bit resolution<br>Conversion target: ANI0～ANI34 | 1.8V≤VDD≤5.5V | 45 | | | Tmclk |
| | | 12-bit resolution<br>Conversion object: internal reference voltage, temperature sensor output voltage, PGA output voltage | 1.8V≤VDD≤5.5V | 72 | | | Tmclk |
| Zero error note 1 | $E_{ZS}$ | 12-bit resolution | 1.8V ≤$AV_{REFP}$ ≤5.5V | | 0 | | LSB |
| Full scale error note 1 | $E_{FS}$ | 12-bit resolution | 1.8V ≤$AV_{REFP}$ ≤5.5V | | 0 | | LSB |
| Integral linearity error note 1 | ILE | 12-bit resolution | 1.8V ≤$AV_{REFP}$ ≤5.5V | -1 | | 1 | LSB |
| Differential linearity error note 1 | DLE | 12-bit resolution | 1.8V ≤$AV_{REFP}$ ≤5.5V | -1.5 | | 1.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0～ANI34 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage (1.8V≤VDD≤5.5V) | | $V_{BGR}$ note2 | | | V |
| | | The output voltage of the temperature sensor (1.8V≤VDD≤5.5V) | | $V_{TMPS25}$ note2 | | | V |

note：1. Does not include quantization error (±1/2 LSB).

2. Please refer to "6.8.2 Characteristic of Temperature Sensor/Internal Reference Voltage"。

3. Tmclk is the AD action clock cycle, the maximum action frequency is 64MHz.

2) Select the case of reference voltage (+)=VDD and reference voltage (-)=VSS

(TA=–40～+105℃, 1.8V≤ VDD≤ 5.5V, VSS=0V, reference voltage (+)=VDD, reference voltage (–)=VSS)

| item | symbol | condition | | MIN. | TYP. | MAX. | unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | 12 | | bit |
| Composite error note 1 | AINL | 12-bit resolution | 1.8V ≤$AV_{REFP}$ ≤5.5V | | 6 | | LSB |
| Conversion time note 3 | $t_{CONV}$ | 12-bit resolution<br>Conversion target: ANI0～ANI34 | 1.8V≤VDD≤5.5V | 45 | | | Tmclk |
| | | 12-bit resolution<br>Conversion object: internal reference voltage, temperature sensor output voltage, PGA output voltage | 1.8V≤VDD≤5.5V | 72 | | | Tmclk |
| Zero error note 1 | $E_{ZS}$ | 12-bit resolution | 1.8V ≤$AV_{REFP}$ ≤5.5V | | 0 | | LSB |
| Full scale error note 1 | $E_{FS}$ | 12-bit resolution | 1.8V ≤$AV_{REFP}$ ≤5.5V | | 0 | | LSB |
| Integral linearity error note 1 | ILE | 12-bit resolution | 1.8V ≤$AV_{REFP}$ ≤5.5V | -2 | | 2 | LSB |
| Differential linearity error note 1 | DLE | 12-bit resolution | 1.8V ≤$AV_{REFP}$ ≤5.5V | -3 | | 3 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0～ANI34 | | 0 | | $V_{DD}$ | V |
| | | Internal reference voltage (1.8V≤VDD≤5.5V) | | $V_{BGR}$ note2 | | | V |
| | | The output voltage of the temperature sensor (1.8V≤VDD≤5.5V) | | $V_{TMPS25}$ note2 | | | V |

note：1. Does not include quantization error (±1/2 LSB).

2. Please refer to "6.8.2 Characteristic of Temperature Sensor/Internal Reference Voltage".

3. Tmclk is the AD action clock cycle, the maximum action frequency is 64MHz.

## 6.8.2 Characteristic of temperature sensor/internal reference voltage

（$T_A$=–40～+105℃、1.8V≤VDD≤5.5V、VSS=0V）

| item | symbol | condition | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|---|
| The output voltage of the temperature sensor | VTMPS25 | ADS register=80H, TA=+25℃ | | 1.09 | | V |
| Internal reference voltage | VBGR | ADS register=81H | 1.38note1 | 1.45 | 1.5note1 | V |
| Temperature Coefficient | FVTMPS | | | -3.5 | | mV/℃ |
| Stable operation waiting time | tAMP | | 5 | | | μs |

note1: Low temperature Specification Value is guaranteed by design, mass production does not measure low temperature conditions.

## 6.8.3 comparator

（$T_A$=–40～+105℃、1.8V≤VDD≤5.5V、$V_{SS}$=0V）

| item | symbol | condition | | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|---|---|
| input deviation voltage | $V_{IOCMP}$ | | | | ±10 | ±40 | mV |
| input voltage range | Ivcmp | | | 0 | | VDD | V |
| Internal reference voltage deviation | $\Delta V_{IREF}$ | CmRVM register: 7FH ~ 80H (m = 0, 1) | | | | ±2 | LSB |
| | | others | | | | ±1 | LSB |
| Response time | tCR, tCF | input amplitude ±100mV | | | 70 | 150 | ns |
| Stable operation $time_{note1}$ | tCMP | CMPn=0->1 | VDD= 3.3 ~ 5.5V | | | 1 | μs |
| | | | VDD= 1.8 ~ 3.3V | | | 3 | |
| Reference voltage stabilization time | tVR | CVRE=0->1 note2 | | | | 20 | μs |
| operating current | $I_{CMPDD}$ | Separately, it is defined as the operation current of peripheral functions. | | | | | |

note1：The time required from the enable of the comparator action (CMPnEN=0 —>1) to meeting the various DC/AC style requirements of CMP.

note2：After the internal reference voltage generator is enabled (by setting the CVREm bit to 1; m = 0 to 1), the comparator output can be enabled after the reference voltage stabilization time (CnOE bit = 1; n = 0 to 1)

## 6.8.4 PGA electrical characteristic

TA=25°C, VDD=5V, VIN+=0.01V, unless otherwise specified. (G is the gain multiple)

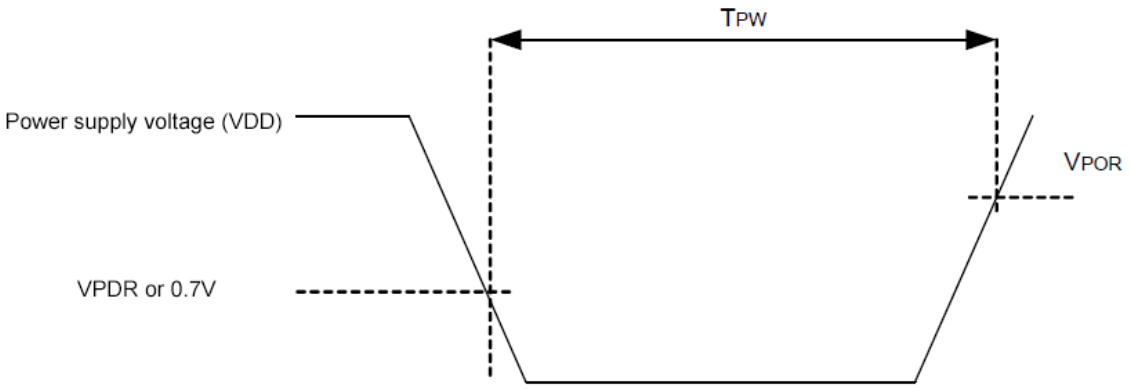
| symbol | parameter | condition | Min value | Typical value | Max value | unit |
|---|---|---|---|---|---|---|
| VDD | voltage | - | 2.5 | - | 5.5 | V |
| $I_Q$ | Quiescent Current | $V_{OUT}$=2V | - | 0.5 | 0.7 | mA |
| $I_{SD}$ | Shutdown current | - | - | 10 | - | nA |
| $T_A$ | Operating temperature | - | -40 | 25 | 105 | ˚C |
| inputcharacteristic | | | | | | |
| $V_{OS}$ | Input offset voltage | Not zero offset (PGAADJ=20H) | - | ±2.5 | - | mV |
| | | Zero offset | - | ±0.1 | ±0.2 | |
| $V_{CM}$ | Common mode input voltage range | G=1 | 0.032 | - | (VDD-1.5)/ G | V |
| | | G=2 | 0.016 | | | |
| | | G=4 | 0.008 | | | |
| | | G=8 | 0.004 | | | |
| | | G=16 | 0.002 | | | |
| | | G=32, 64,128 | 0.001 | | | |
| $I_B$ | input bias current | - | - | 10 | - | pA |
| $I_{OS}$ | Input offset current | - | - | 10 | - | pA |
| Output characteristic | | | | | | |
| EG | Gain error | G=1, 2, 4, 8, 16 | -1 | - | 1 | % |
| | | G=32 | -2 | - | 2 | |
| | | G=64,128 | -4 | - | 4 | |
| $C_{LOAD}$ | Capacitive load | - | - | 10 | - | pF |
| $V_{OH}$ | Maximum output voltage | -40˚C~105˚C | - | - | VDD-1.5 | V |
| $V_{OL}$ | Minimum output voltage | -40˚C~105˚C | 0.032 | - | - | V |
| Frequency characteristic | | | | | | |
| BW | bandwidth | $C_{LOAD}$=10pF,G=1 | - | 1.5 | - | MHz |
| PSRR | Power supply rejection ratio | VDD=2.5~5.5V,G=16 | - | 75 | - | dB |
| CMRR | Common mode rejection ratio | -40˚C~105˚C | - | 80 | - | dB |
| Transient characteristic | | | | | | |
| SR | Slew rate | $C_{LOAD}$=10pF,G=32 | - | 10 | - | V/μs |
| $T_{STB}$ | stable time | - | - | - | 2 | μs |
| $T_{SH(1)}$ | Sampling hold time | - | - | 3 | - | μs |

## 6.8.5 POR circuit characteristic

（$T_A$=–40～+105℃、$V_{SS}$=0V）

| item | symbol | condition | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|---|
| Detection voltage | VPOR | When the power supply voltage rises | | 1.60 | 1.75 | V |
| | VPDR | When the power supply voltage drops | 1.37 | 1.50 | 1.55 | V |
| Minimum pulse width[note1] | TPW | | 300 | | | μs |

note1.：This is the time required for POR to reset when VDD is lower than VPDR. In addition, in the deep sleep mode, when the main system clock (fMAIN) is stopped by setting bit0 (HIOSTOP) and bit7 (MSTOP) of the clock operation status control register (CSC), the oscillation of the main system clock (fMAIN) is stopped from VDD lower than 0.7V to rise above VPOR. Time required for POR reset.



## 6.8.6 LLVD circuit characteristic

1) Reset mode and interrupt mode

（$T_A$=–40～+105℃、$V_{PDR}$≤$V_{DD}$≤5.5V、$V_{SS}$=0V）

| item | symbol | condition | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|---|
| Detection voltage | VLVD0 | power supply voltage rises | | 4.06 | | V |
| | | power supply voltage drops | | 3.98 | | V |
| | VLVD1 | power supply voltage rises | | 3.75 | | V |
| | | power supply voltage drops | | 3.67 | | V |
| | VLVD2 | power supply voltage rises | | 3.13 | | V |
| | | power supply voltage drops | | 3.06 | | V |
| | VLVD3 | power supply voltage rises | | 3.02 | | V |
| | | power supply voltage drops | | 2.96 | | V |
| | VLVD4 | power supply voltage rises | | 2.92 | | V |
| | | power supply voltage drops | | 2.86 | | V |
| | VLVD5 | power supply voltage rises | | 2.81 | | V |
| | | power supply voltage drops | | 2.75 | | V |
| | VLVD6 | power supply voltage rises | | 2.71 | | V |
| | | power supply voltage drops | | 2.65 | | V |
| | VLVD7 | power supply voltage rises | | 2.61 | | V |
| | | power supply voltage drops | | 2.55 | | V |
| | VLVD8 | power supply voltage rises | | 2.50 | | V |
| | | power supply voltage drops | | 2.45 | | V |
| | VLVD9 | power supply voltage rises | | 2.09 | | V |
| | | power supply voltage drops | | 2.04 | | V |
| | VLVD10 | power supply voltage rises | | 1.98 | | V |
| | | power supply voltage drops | | 1.94 | | V |
| | VLVD11 | power supply voltage rises | | 1.88 | | V |
| | | power supply voltage drops | | 1.84 | | V |
| Minimum pulse width | tLW | | 300 | | | μs |
| Detection delay | | | | | 300 | μs |

2) Interrupt and reset mode

（$T_A$=–40～+105℃、$V_{PDR}$ ≤$V_{DD}$≤5.5V、$V_{SS}$=0V）

| item | symbol | condition | | | MIN. | TYP. | MAX. | unit |
|---|---|---|---|---|---|---|---|---|
| Interrupt & reset mode | $V_{LVDA0}$ | $V_{POC2}$、$V_{POC1}$、$V_{POC0}$=0、0、0, Decrease reset voltage | | | | 1.63 | | V |
| | $V_{LVDA1}$ | | LVIS1、LVIS0=1、0 | rising reset release voltage | | 1.77 | | V |
| | | | | drop interrupt voltage | | 1.73 | | V |
| | $V_{LVDA2}$ | | LVIS1、LVIS0=0、1 | rising reset release voltage | | 1.88 | | V |
| | | | | drop interrupt voltage | | 1.84 | | V |
| | $V_{LVDA3}$ | | LVIS1、LVIS0=0、0 | rising reset release voltage | | 2.92 | | V |
| | | | | drop interrupt voltage | | 2.86 | | V |
| | $V_{LVDB0}$ | $V_{POC2}$、$V_{POC1}$、$V_{POC0}$=0、0、1，decrease reset voltage | | | | 1.84 | | V |
| | $V_{LVDB1}$ | | LVIS1、LVIS0=1、0 | rising reset release voltage | | 1.98 | | V |
| | | | | drop interrupt voltage | | 1.94 | | V |
| | $V_{LVDB2}$ | | LVIS1、LVIS0=0、1 | rising reset release voltage | | 2.09 | | V |
| | | | | drop interrupt voltage | | 2.04 | | V |
| | $V_{LVDB3}$ | | LVIS1、LVIS0=0、0 | rising reset release voltage | | 3.13 | | V |
| | | | | drop interrupt voltage | | 3.06 | | V |
| | $V_{LVDC0}$ | $V_{POC2}$、$V_{POC1}$、$V_{POC0}$=0、1、0，decrease reset voltage | | | | 2.45 | | V |
| | $V_{LVDC1}$ | | LVIS1、LVIS0=1、0 | rising reset release voltage | | 2.61 | | V |
| | | | | drop interrupt voltage | | 2.55 | | V |
| | $V_{LVDC2}$ | | LVIS1、LVIS0=0、1 | rising reset release voltage | | 2.71 | | V |
| | | | | drop interrupt voltage | | 2.65 | | V |
| | $V_{LVDC3}$ | | LVIS1、LVIS0=0、0 | rising reset release voltage | | 3.75 | | V |
| | | | | drop interrupt voltage | | 3.67 | | V |
| | $V_{LVDD0}$ | $V_{POC2}$、$V_{POC1}$、$V_{POC0}$=0、1、1，decrease reset voltage | | | | 2.75 | | V |
| | $V_{LVDD1}$ | | LVIS1、LVIS0=1、0 | rising reset release voltage | | 2.92 | | V |
| | | | | drop interrupt voltage | | 2.86 | | V |
| | $V_{LVDD2}$ | | LVIS1、LVIS0=0、1 | rising reset release voltage | | 3.02 | | V |
| | | | | drop interrupt voltage | | 2.96 | | V |
| | $V_{LVDD3}$ | | LVIS1、LVIS0=0、0 | rising reset release voltage | | 4.06 | | V |
| | | | | drop interrupt voltage | | 3.98 | | V |

### 6.8.7 The rising slope of the power supply voltage characteristic

（$T_A$=–40～+105℃、$V_{SS}$=0V）

| item | symbol | condition | MIN | TYP | MAX | unit |
|---|---|---|---|---|---|---|
| The rising slope of the power supply voltage | SVDD | | | | 54 | V/ms |

# 6.9 Memory characteristic

## 6.9.1 Flash Memory

（$T_A$=–40～+105° C、1.8V≤EVDD=VDD≤5.5V、$V_{SS}$=$EV_{SS}$=0V）

| Symbol | Parameter | Conditions | MIN | MAX | Unit |
|---|---|---|---|---|---|
| Tprog | Word Program(32bit) | Ta=–40～+105℃ | 24 | 30 | μs |
| Terase | Sector erase(512B) | Ta=–40～+105℃ | 4 | 5 | ms |
| | Chip erase | Ta=–40～+105℃ | 20 | 40 | ms |
| $N_{END}$ | Endurance | Ta=–40～+105℃ | 100 | | kcycle |
| tRET | Data retention | 100 kcycle(note2) at Ta = 105℃ | 20 | | Years |

Note1：Data based on characterization results, not tested in production.

Note2：Cycling performed over the whole temperature range.

## 6.9.2 RAM Memory

（$T_A$=–40～+105° C、1.8V≤EVDD=VDD≤5.5V、$V_{SS}$=$EV_{SS}$=0V）

| Symbol | Parameter | Conditions | MIN | MAX | Unit |
|---|---|---|---|---|---|
| $V_{ramhold}$ | RAM Hold Voltage | Ta=–40～+105℃ | 0.8 | | V |

# 6.10 Electrical sensitivity characteristic

## 6.10.1 Electrostatic discharge (ESD)

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | TA = +25°C, conforming to JESD22-A114 | 3A |

Note：Data based on characterization results, not tested in production.

## 6.10.2 Static latch-up(LU)

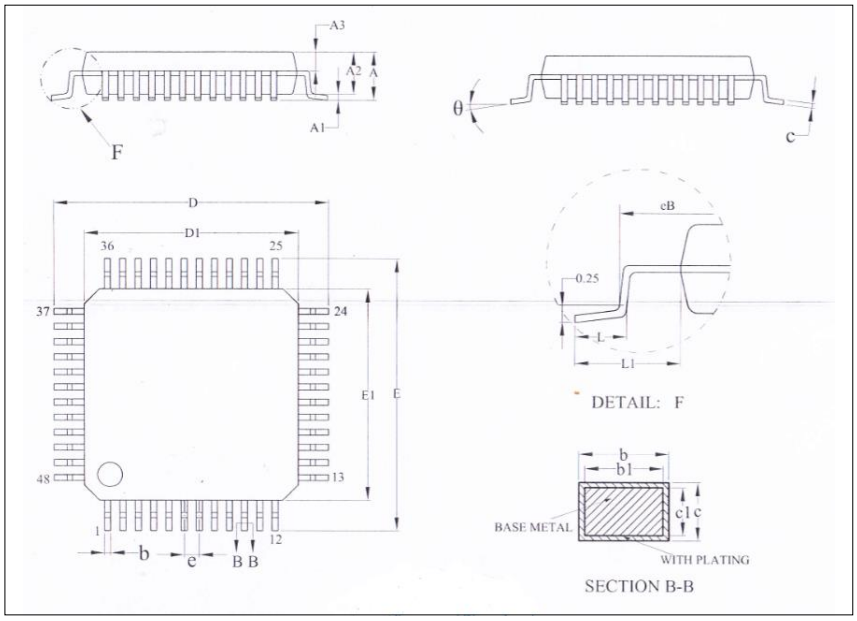
| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | TA = +25°C conforming to JESD78E | I levelA |

Note：Data based on characterization results, not tested in production.

# 7 Package size chart

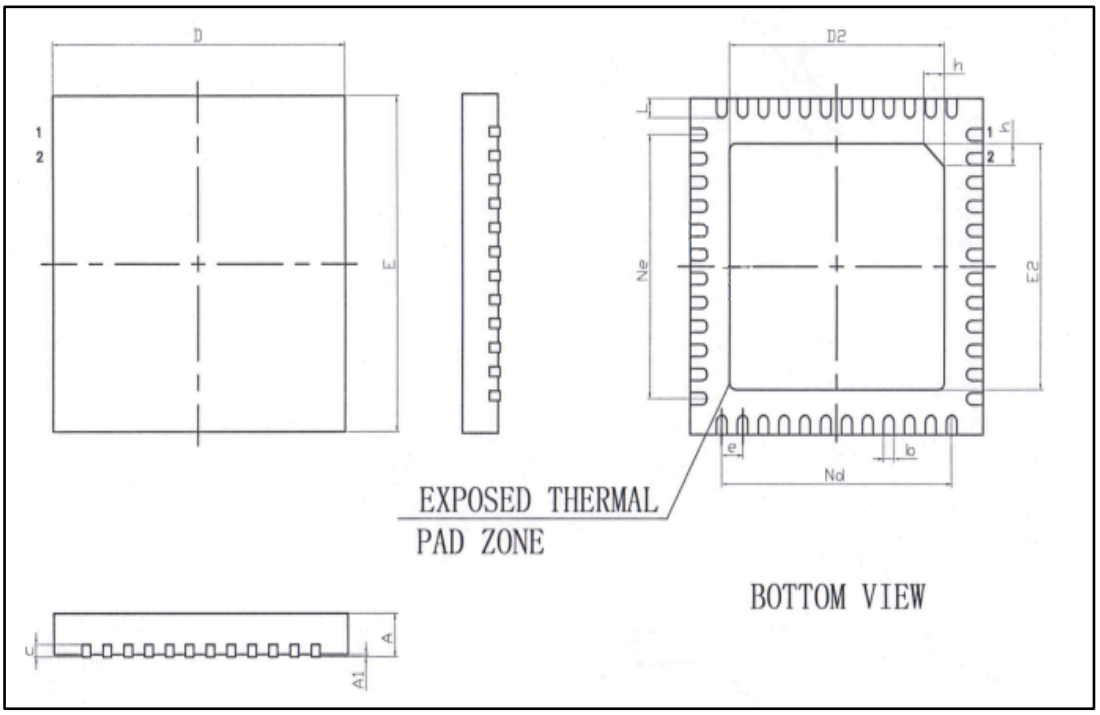
## 7.1 48 pin product

48LQFP（7x7mm，0.5mm spacing）




| Symbol | Millimeter | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | - | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | - | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| eB | 8.10 | - | 8.25 |
| e | 0.50BSC | | |
| L | 0.45 | - | 0.75 |
| L1 | 1.00REF | | |
| θ | 0 | - | 7° |

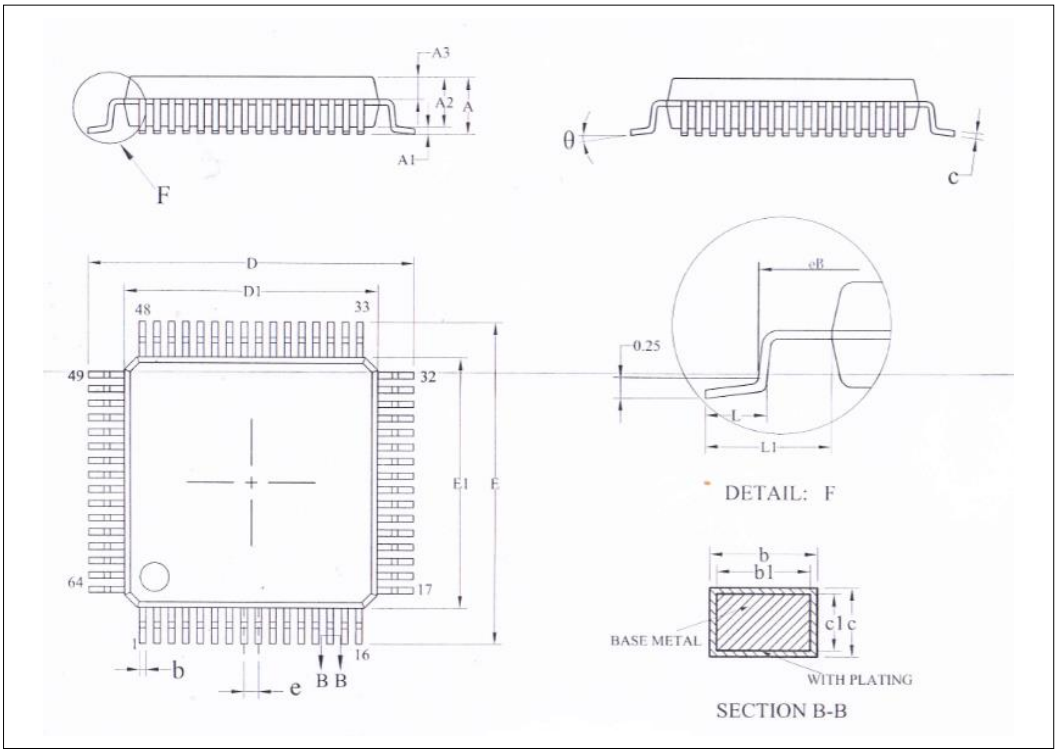
48QFN（6x6mm，0.4mm spacing）




| Symbol | Millimeter | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 |
| A1 | - | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.18 | 0.20 | 0.23 |
| D | 5.90 | 6.00 | 6.10 |
| D2 | 4.10 | 4.20 | 4.30 |
| e | 0.40BSC | | |
| Nd | 4.40BSC | | |
| Ne | 4.40BSC | | |
| E | 5.90 | 6.00 | 6.10 |
| E2 | 4.10 | 4.20 | 4.30 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.30 | 0.35 | 0.40 |

## 7.2 64 pin product

64LQFP（7x7mm，0.4mm spacing）




| Symbol | Millimeter | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.16 | - | 0.24 |
| b1 | 0.15 | 0.18 | 0.21 |
| c | 0.13 | - | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| eB | 8.10 | - | 8.25 |
| e | 0.40BSC | | |
| L | 0.45 | - | 0.75 |
| L1 | 1.00REF | | |
| θ | 0 | - | 7° |

# 8 Modify resume

| Rev. | Release date | Content modified | |
|---|---|---|---|
| | | Page/section | content |
| V1.0 | 2020/11/4 | - | Original Issue |
| V1.1 | 2020/11/10 | - | Update PGA characteristic |
| V1.2 | 2020/12/16 | - | Update pin diagram |
| V1.3 | 2021/01/19 | | Update format |
| V1.4 | 2021/02/01 | 6.5.2 | Update Mistakes |
| V1.5 | 2021/04/14 | 6.4.2, 6.8.2 | Add low temperature condition note explanation |
| V1.6 | 2021/06/10 | 4.1, 4.2<br>- | Modify the pin function description<br>Correct the misrepresentation of SSIE |
| V1.7 | 2021/06/22 | 4.1 | Update Mistakes |
| V1.8 | 2021/12/14 | 2, 6.5 | Update Mistakes |
| V1.9 | 2022/01/12 | 6.5 | Update Mistakes |
| V2.0 | 2022/02/11 | 1.3, 7.1 | Add BAT32G157GK48NB describe |
| V2.01 | 2023/02/13 | 6.10.1 | Delete the maximum value and level |